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A Study of Direct Digital Manufactured RF/Microwave Packaging

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A Study of Direct Digital Manufactured

RF/Microwave Packaging

by

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A thesis submitted in partial fulfillment
of the requirements for the degree of
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Thermal, Wilkinson

DEDICATION

To my wife, Lindsey, who has loved me unconditionally throughout my academic career, endless as it has sometimes seemed.

To my parents, all four of them, who have seemingly endless supplies of support and encouragement.

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I am extremely grateful to Dr. Thomas Weller for affording me the opportunity to complete graduate school whilst working on something new and exciting. His constant guidance and advice has made it possible for me to succeed, and his tireless commitment to his profession is an inspiring example of how one should pursue success.

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ABSTRACT

Various facets of direct digital manufactured (DDM) microwave packages are studied. The rippled surface inherent in fused deposition modeling (FDM) fabricated geometries is modeled in Ansoft HFSS, and its effect on the performance of microstrip transmission lines is assessed via simulation and measurement. The thermal response of DDM microstrip transmission lines is analyzed over a range of RF input powers, and linearity is confirmed over that range.

Two IC packages are embedded into DDM printed circuit boards, and their performance is analyzed. The first is a low power RF switch, and the second is an RF front end device that includes a low noise amplifier (LNA) and a power amplifier (PA). The RF switch is shown to perform well, as compared to a layout designed for a Rogers 4003C microwave laminate substrate. The LNA performs within datasheet specifications. The power amplifier generates substantial heat, so a thermal management attempt is described.

Finally, a capacitively loaded 6dB Wilkinson power divider is designed and fabricated using DDM techniques and materials. Its performance is analyzed and compared to simulation. The device is shown to compare favorably to a similar device fabricated on a Rogers 4003C microwave laminate using traditional printed circuit board techniques.

CHAPTER 1: INTRODUCTION

In the 1990's, monolithic microwave integrated (MMIC) technology was beginning to mature [2], and the benefits and profitability of this technology were causing a great deal of industry excitement. With the advent of this technology came the inevitable search for compatible high performance packaging solutions. Packaging is indeed an issue for all electronics, but the issue is much more complex when dealing with RF/microwave devices [3] where substrate surface roughness, trace dimensions, etc., all significantly impact performance. There are several key performance characteristics which must be met when developing microwave package solutions. These include mechanical considerations, such as the ability to support temperature cycling and vibrations, as well as electrical considerations such as RF losses in, and the ability to control the RF impedance of, interconnects [3].

3D printing is a term which is becoming ever more abundant in today's vernacular. While this technology has been around for over 20 years [4] it is relatively recent that commercially available consumer grade printers have entered the market. 3D printing is a generic term for an additive manufacturing technology, but there are several names. In this thesis, the term direct digital manufacturing (DDM) is used, as this term has a broader scope, and can be used to describe the additive manufacturing of complex 3D structures, as well as the direct printing of single layer geometries, like conductive traces, onto a given surface.

As the interest in DDM grows, the scope of its application invariably grows with it. This thesis is a study of its application to RF/microwave circuits, and the feasibility of packaging functional RF electronics into 3D geometries, using a single platform.

1.1 Thesis Overview and Contributions

The principal purpose of this thesis is to evaluate the electrical and thermal performance of a particular sub-set of DDM RF/microwave packaging materials. There are many emerging techniques, technologies, and materials in the realm of direct digital manufacturing. This thesis deals specifically with RF circuits fabricated using 3D printed Acrylonitrile Butadiene Styrene (ABS) substrates with DuPont CB028 conductive traces printed directly on the substrate. For thermal management and the bonding of surface mount components to the circuit, H20E, a two-part conductive epoxy is used. This fabrication process is achieved in a single process using an nScrypt 3Dn-300™ printer. This system uses the nScrypt nFD™ process, a fused deposition modeling (FDM) technology designed for the fine extrusion of ABS and the nScrypt SmartPump™ for the printing of the conductive ink.

A fundamental limitation of DDM using the FDM approach is the resolution of the print. As will be detailed in Chapter 2, the FDM process involves the extrusion of ABS via a heated nozzle. 3D structures are produced this way by depositing lines of molten plastic in the x-y plane, repeatedly while moving in incremental steps up along the z-axis. This line-by-line approach leads to a rippled surface pattern, which is not ideal for an RF substrate. An analysis of the effect of this characteristic on RF performance is the first major contribution of this thesis, and is presented in Chapter 4. Also presented in Chapter 4 is a study of the thermal response of a DDM fabricated microstrip line with a high power RF input.

The second major contribution of this thesis is the embedding of IC device packages into a DDM fabricated printed circuit board (PCB), and an initial attempt at a thermal management solution. Chapter 5 presents a study into the performance of two IC packaged components used on a DDM fabricated PCB. The first is an RF switch in an SC-70 package, and the second is a 2.45 GHz RF front end device, which includes a low noise amplifier (LNA) and a power amplifier (PA)

in a single UQFN-16 package. These two packaging types were chosen because they offer two common types of device connections. The SC-70 has 6 leads emanating from the device, while the UQFN-16 has small pads on the underside of the chip, as well as a large ground pad used for thermal management. This thermal management issue is a major concern for active devices, so a first attempt at solving the issue using traditional techniques and DDM compatible materials is presented.

The third major contribution of this thesis is the design and implementation of a DDM fabricated 6dB capacitively loaded Wilkinson power divider. This work is presented in Chapter 6, which begins with a summary of the theory of operation of a Wilkinson power divider, as well as a miniaturization technique that uses capacitive loading. In section 6.4, traditionally fabricated 3dB and 6dB capacitively loaded Wilkinson power dividers on Rogers 4003C microwave laminate are presented. Then in section 6.5, DDM fabricated 3dB and 6dB capacitively loaded Wilkinson power dividers are presented, and the performance is compared to the Rogers 4003C versions.

Chapter 7 summarizes and concludes the findings presented in the thesis, and offers suggestions for further study in these areas.

CHAPTER 2: DIRECT DIGITAL MANUFACTURING BACKGROUND

2.1 Introduction

Direct digital manufacturing (DDM) is an additive manufacturing method which fabricates a 3D part directly from a digital 3D model, which may come in the form of a CAD file, for example [5]. A consensus has not yet been reached as to what to name this technology, so other names such as "Direct Print Additive Manufacturing (DPAM)," "rapid manufacturing" or simply the generic "3D printing" are often used. It is important to note that "rapid manufacturing" is only part of the DDM story as DDM offers more than an increase in speed. DDM fundamentally changes the manufacturing landscape, making possible the previously impossible. It is for this reason that DDM has been called the next industrial revolution [5].

When designing a part to be manufactured using traditional methods, such as injection molding, casting, or machining, one is constrained to an "outside-in" approach. Machining involves the stripping away of material to leave the desired geometry, and injection molding requires a mold in which to inject a material. There are clear physical limitations to these approaches. These limitations are avoided with DDM, since the part is built from scratch, using a layer-by-layer "inside-out" approach. The complexity of geometries that are producible with this technology is far greater, and there is no need for expensive molds or fixtures. High quality consumer grade DDM technology exists now, such as the Printrbot Play, which is available for around $400 [6].

By combining multiple materials into a single geometry, the spectrum of realizable products increases. Combining high conductivity materials with plastics, for example, allow the creation of sturdy 3D geometries with embedded functional electronics. With this approach, the retro-fitting of

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electronic components and PCBs into a structure becomes unnecessary. Printable electronics have been a topic of significant interest, since this potentially broadens the scope of materials onto which electronics can be secured. Flexible electronics, for example, are produced by printing conductive ink traces onto thin, flexible dielectric substrates. Combining additive manufacturing and micro-dispensing technologies in a single platform allows the single process production of structurally sound 3D geometries with embedded functional electronics.

In section 2.2, the fused deposition modeling (FDM) additive manufacturing technique is described, and some benefits and limitations are discussed. In section 2.3, the direct-write technique for the printing of electronic conductors is described, and some benefits and limitations are discussed.

2.2 Fused Deposition Modeling (FDM)
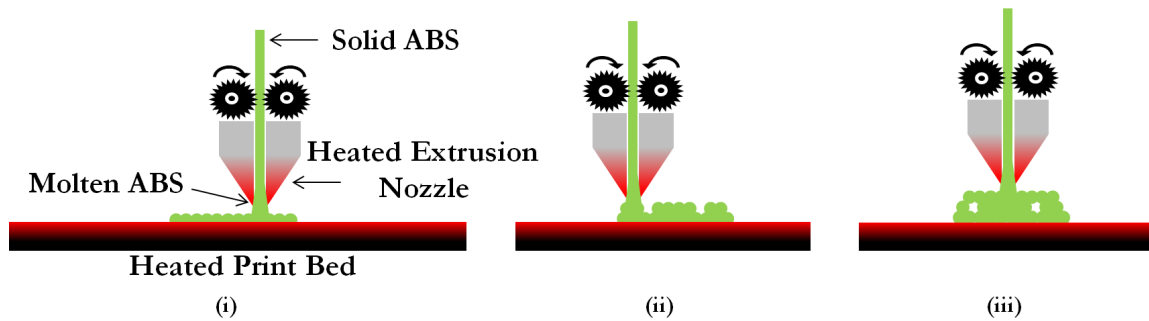
Figure 2.1 FDM print process. (i) An initial layer of molten plastic is extruded onto a heated bed. (ii) The print head moves up and the second layer is printed. (iii) The print head moves up, and the third layer is printed.

Fused deposition modeling (FDM) is an additive manufacturing technique whereby three dimensional parts are built layer-by-layer using molten Acrylonitrile Butadiene Styrene (ABS), or some other compatible thermo-plastic [1]. In this process ABS filament is fed through a nozzle that is heated to around 230°C, which melts the ABS. The molten ABS is then deposited onto a surface as the print head moves in the x-y plane. By repeating this process with incremental steps in the +z direction, a 3D part is fully formed [1] This process is depicted in Figure 2.1. It is good practice for

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the print-bed to be heated to around 90°C to improve adhesion of the part to the bed, and prevent premature peeling or warping [7]. This heated bed, as shall be discussed in section 2.3, has an ancillary benefit when also printing conductive traces.

ABS has a glass transition temperature (GTC) of around 105°C, depending on the brand [7].The GTC is the temperature at which an amorphous material transitions from a solid state to a molten state. This transition is reversible with cooling. This temperature is the upper limit of what could be considered the useful operating temperature of ABS.
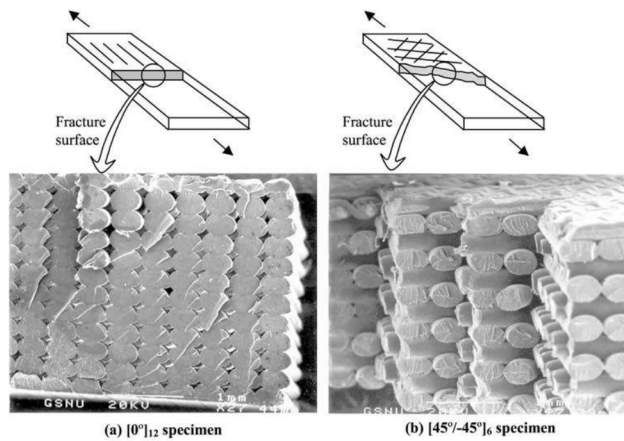
Figure 2.2 Cross section cuts of an FDM printed part [1]. Permission included in Appendix A.

A fundamental limitation of this printing process is the resolution of the print. Since the print is constructed of what could simplistically be described as set of fused plastic cylinders, there is an inherent roughness to the print. A cross section cut of an FDM print is shown in Figure 2.2. Here it is clear that the surface and internal structure has something of a rippled effect, due to the thermal fusing of parallel ABS cylinders. The resolution of the print is determined by the inner diameter of the print-head nozzle. Consumer FDM devices, such as the MakerBot Replicator, have print resolutions of around 100μm, which is to say that each printed bead has a height of approximately 100 μm [8]. More advanced systems, such as nScrypt's nFD™ print head are capable

of print resolutions as low as 12.5 μm [9]. The nScrypt nFD ™ tool is used for the work presented in this thesis. For RF applications, this print resolution is important, as will be seen in Chapter 4.

2.3 Direct-Write Printing
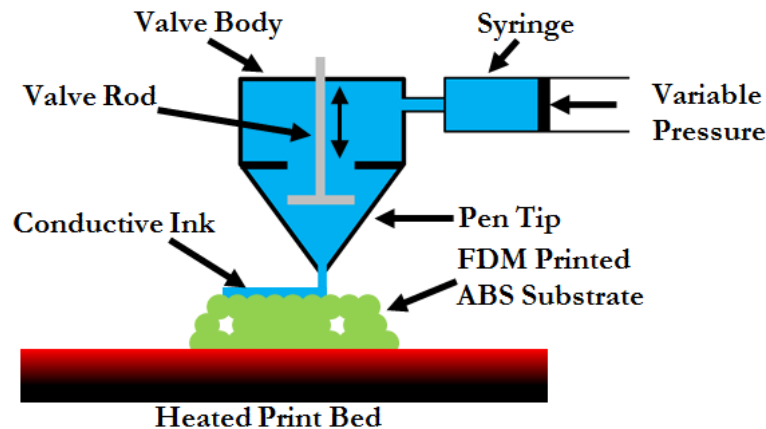
Figure 2.3 Direct-write printing process.

Functional 3D electronic structures have two fundamental components, the dielectric structural component, and the conductive trace component. FDM is one method used for the former, and the latter may be achieved through a direct-write process. Direct-write is a process whereby conductive inks are printed directly onto a surface, and then hardened via some curing method. For the work presented in this thesis, nScrypt's SmartPump™ technology is used for printing conductive traces on top of FDM printed ABS substrates. The SmartPump™ is capable of producing printed line widths as low as 20 μm [10] and can print repeatable dots and lines through its precise volumetric output control. Figure 2.3 shows a simplified diagram of the SmartPump™ operation. The material to be printed is loaded into a syringe, and the syringe tip is connected to the valve body. Air pressure is applied to the stopper in the syringe, and this pressure is precisely controllable through the system software. This is the first means of controlling the volumetric output. A second output control is provided by a retractable valve rod which can be moved up and

down in very precise increments to control the amount of material that can flow through the pen tip.

The conductive material of choice for the work presented in this thesis is DuPont CB028, which is an Ag microparticle based conductive paste. CB028 requires thermal curing, and the conductivity of the cured ink is heavily dependent on the curing temperature [11]. The CB028 data sheet recommends curing at 160°C for 60 minutes to reach an optimal sheet resistivity of 7-10 mΩ/sq/mil. This temperature is too high since this is much greater than the GTC of ABS. However [11] shows that there is no appreciable increase in resistivity if cured at around 95°C for 1 hour. This is ideal since the FDM printed part sits on a print bed which is heated to around 90°C. This allows the in-situ curing of the CB028, which makes the single platform fabrication of functional 3D electronic structures possible.

CHAPTER 3: MICROWAVE PACKAGING BACKGROUND

3.1 Introduction

The purpose of this thesis not to design a new packaging technology for microwave devices, but rather to evaluate the quality of microwave packages that can be produced using a particular set of DDM techniques and materials. Since the silicon boom of the 1950s, the development of electronics packaging has largely focused on the packaging of integrated circuit (IC) devices, which tend to be incredibly small [12]. This trend, though, does not form the definition of electronics packaging. This thesis is not about the DDM fabrication of packaging for IC devices, but more generally for RF sub-systems that include distributed elements as well as pre-packaged IC components. In [12] a packaging hierarchy is defined. Level 0 of this hierarchy is defined as the gate-to-gate interconnects on a Si chip. The highest level, level 5, is defined as connections between independent, physically separated systems, such as a computer and printer. The packaging studied in this thesis is most closely related to level 2, the printed circuit board (PCB). The PCB electrically connects various electrical components through conductive traces embedded in a dielectric substrate, provides a means to remove heat generated by a component, and provides a means to connect the PCB to external devices, for power or communication [12].

The primary purpose of electronics packaging is to provide a means to electrically connect electronic components, mechanically secure them, separate them from their environment, and thermally manage them. These ends must be achieved in such a way that does not appreciably affect the performance of the circuit [2]. The electrical and thermal performance of electronics packaging is discussed in the following sections. The effect that the package has on the performance of low

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frequency electronics is typically much less significant than for high frequency electronics, where the sizes and shapes of conductors matter, and parasitic inductances and capacitances begin to affect the electrical performance.

3.2 Electrical Performance

The RF/microwave package must be capable of interfacing RF and DC between itself and something external [2]. Ideally, the package would not introduce additional noise to the RF signal, or degrade the quality of the signal in any way. This, of course, is not an attainable goal, so the degradation of the signal must be minimized to the extent possible. For RF signals, the ability to control the characteristic impedance of a transmission line is important [3], since minimizing signal reflections minimizes both the noise figure and the insertion loss of the transmission line.

The electrical properties of the materials used in the package have significant impact on the performance. Dielectric materials with high loss tangents and conductive materials with low conductivity will cause a signal to be attenuated as it propagates through the system. At low frequencies, the loss in the conductor dominates, but as frequency increases the loss in the dielectric material increases, and eventually dominates [12]. This not only reduces the power of the signal, but increases the noise figure of the system.

The noise figure of a system, which is a measure of the change in signal-to-noise ratio between the input and output terminals of the system, is an important design consideration, and is impacted by both of the factors mentioned above; the quality of matching and the attenuation of a signal. This effect can be shown mathematically. Considering a lossy transmission line of characteristic impedance Z_T in a system designed for characteristic impedance Z_0, as depicted in Figure 3.1, where L represents the loss on the line, it is clear that if $Z_T \neq Z_0$, then $\Gamma_S \neq 0$ and $\Gamma_L \neq 0$. The effect of this on the noise figure, F, is demonstrated in [13] and is summarized below.

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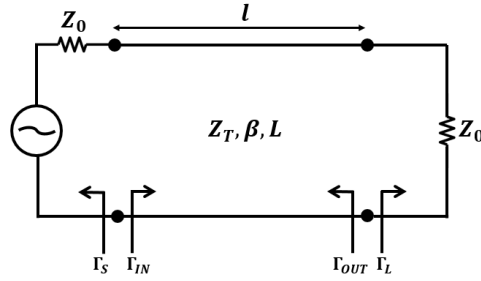
Figure 3.1 Transmission line of characteristic impedance Z_T in a system designed for characteristic impedance Z_0.

Equation 3.1 gives the S-parameter matrix for a lossy transmission line, referenced to characteristic impedance Z_T. Substituting the appropriate values from equation 3.1 into equation 3.2, which gives the expression for Γ_{OUT}, yields equation 3.3.

$$[S]_{Z_T} = \frac{e^{-j\beta l}}{\sqrt{L}} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{3.1}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{3.2}$$

$$\Gamma_{OUT} = \frac{\Gamma_S}{L} e^{-2j\beta l} \tag{3.3}$$

The available power gain of a network, G_{21}, defines how much power is available at port 2 with respect to the power available from the source. The equation for this quantity is given in equation 3.4.

$$G_{21} = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2(1 - |\Gamma_{OUT}|^2)} \tag{3.4}$$

Substitution of the appropriate values from equation 3.1 and equation 3.3 into equation 3.4, and simplifying yields

$$G_{21} = \frac{L(1 - |\Gamma_S|^2)}{L^2 - |\Gamma_S|^2} \tag{3.5}$$

An equation for the equivalent noise temperature of a network, T_e, is

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$$T_e = \frac{1 - G_{21}}{G_{21}} T \tag{3.6}$$

where T is the actual temperature in which the network is operating. Substituting equation 3.5 into equation 3.6 yields

$$T_e = \frac{(L-1)(L+|\Gamma_S|^2)}{L(1-|\Gamma_S|^2)} T \tag{3.7}$$

An expression for the noise figure, F, of a network is

$$F = 1 + \frac{T_e}{T_0} \tag{3.8}$$

So substituting equation 3.7 into equation 3.8 yields the noise figure of a mismatched lossy transmission line at temperature $T = T_0$. The result of this is

$$F = 1 + \frac{(L-1)(L+|\Gamma_S|^2)}{L(1-|\Gamma_S|^2)} \tag{3.9}$$

From this result, it is observed that a lossless and matched transmission line, where $L = 1$ and $\Gamma_S = 1$, the noise figure is simply 1, as expected. That is to say that under this perfect circumstance the transmission line does not introduce any additional noise to the network, which is the ideal case. As the loss of the line and mismatch increases, though, the noise figure increases, so it is important that the packaging technology is able to accommodate a designed characteristic impedance, and minimize the amount of loss in the line. Figure 3.2 shows this equation plotted for L and $|\Gamma_S|$, which demonstrates the extents to which the noise figure is affected with these parameters.

3.3 Thermal Performance

The thermal performance of an electronics package is also of great importance, for several reasons. If the package is to house an active device, such as a power amplifier, then the package must provide a means to dissipate the heat generated by the device. These devices, like any device,

have an operational temperature range, so it is important that the temperature of the device does not surpass the highest temperature in the range.
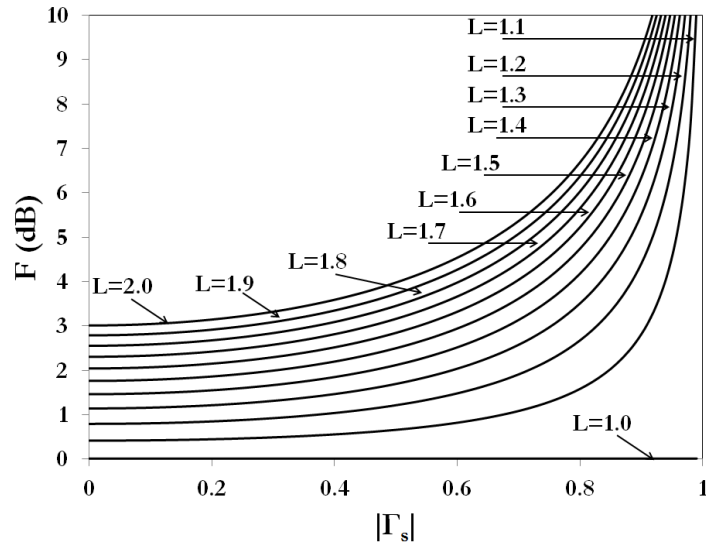
Figure 3.2 Noise Figure (F (dB)) vs. $|\Gamma_s|$ for transmission lines of various loss factor, L.

The materials surrounding the device must also be capable of withstanding the temperatures generated by the device. A material with a low glass transition temperature, for example, may not be suitable for packaging devices whose operating temperatures exceed the GTC. A package that becomes molten when the device is operating is obviously a poor package choice. To minimize the raise in temperature of the materials due to the power dissipated as heat by the active device, the heat must be effectively dissipated. In order to dissipate heat effectively, the packaging technology must be compatible with materials of a sufficiently high thermal conductivity [2], so that heat can be efficiently drawn away from the device. The thermal conductivity of a material, k, which has units of W/mK , is a material property which is used to define the rate at which heat is transferred through a medium. Thermal conduction is defined by Fourier's Law, which is the rate equation

$$q = -Ak\frac{dT}{dx} \quad \text{(Watts)} \tag{3.10}$$

where A is the isothermal cross sectional area of the plane perpendicular to the direction of heat flow, and T is temperature. This equation states that given a temperature gradient across a material

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with thermal conductivity k and cross sectional area A, heat energy will be transferred through the material at a rate of q joules per second. The minus sign accounts for the fact that heat flows from hot to cold [14]. This concept is depicted in Figure 3.2. Given these relationships, it is apparent that in order to efficiently remove heat from a device, a high thermal conductivity material is required.

Another important thermal consideration in electronics packaging is the thermal coefficient of expansion (CTE). More specifically it is important that materials in close proximity have well matched CTEs [15]. CTE defines the extent to which a material expands with temperature. If two materials are in close proximity, and expand with temperature at different rates, then stress is introduced into the body, and the structure may be damaged [12].
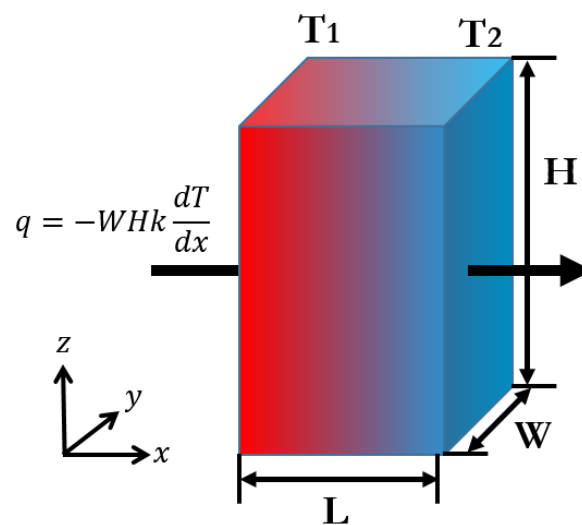
Figure 3.3 Three-dimensional heat transfer by conduction.

Active devices are not the sole source of heat in an electronics package. As discussed in section 3.2, signals will be attenuated as they propagate through a material. Conservation of energy states that the power lost from the signal must be accounted for, which indeed it is, as heat. A dielectric material, in the presence of an electric field, will polarize to some extent [13]. In the presence of an oscillating electric field, this polarization direction is switched back and forth, which generates heat through friction. The conductivity of a material is proportional to the mean time

between collisions of electrons in the material, under the influence of an electric field [16]. When electrons collide, the kinetic energy of the electron is lost as heat. So, a material with high conductivity has longer mean time between collisions, and thus fewer collisions per unit time, which results in less energy lost per unit time (the definition of a Watt), and less heat is generated.

3.4 Conclusion

Electronics packaging should be designed such that its presence has minimal effect on the performance of the circuit. An important consideration when developing electronics packaging, especially RF/microwave packaging, is the materials used, as these have significant effects on the electrical and thermal performance of the system. In this thesis, the conductor materials are of relatively low electrical and thermal conductivity, compared to Cu. The dielectric used has a relatively low loss tangent of around 0.0078, which makes it useful for RF applications, but it has a low GTC, as discussed in Chapter 2. The low GTC of the dielectric and the low conductivity of the conductors mean that there are some thermal limitations to these packaging materials, and this is investigated in detail in this thesis.

CHAPTER 4: MICTROSTRIP INTERCONNECTS

4.1 Introduction

The study of DDM fabricated RF packaging begins with the evaluation of the electrical and thermal performance of microstrip transmission lines. Microstrip transmission lines are common in microwave circuits as this type of line lends itself to PCB geometries[17]. A common technique for microstrip PCB fabrication is to chemically etch copper away from a copper clad substrate, using masks in the shape of the circuit layout. This, of course, is an example of subtractive manufacturing. This thesis focuses on DDM fabricated RF/microwave circuits, whereby a dielectric substrate is printed using FDM, and then the conductive traces are printed directly onto the substrate, and cured in-situ.

This chapter begins with the electrical and thermal simulation of microstrip lines using the electrical and thermal properties of the materials. An important feature of an FDM substrate is the profile of the surface, which is rippled. The electrical response to this surface is studied in detail.

The second half of the chapter deals with electrical and thermal measurements of microstrip lines fabricated using DDM techniques. The measured and simulated results are compared.

4.2 Microstrip Modeling

The nature of FDM imposes a limitation on the surface roughness of a substrate. The surface of substrates manufactured using FDM techniques can be modelled as a series of cylinders, lying parallel to each other, along a given axis. These surface cylinder configurations shall henceforth be referred to as "surface ripple." The question arises as to whether or not the orientation of a microstrip line with respect to the direction of this surface ripple has any appreciable effect on

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performance. Three surface ripple orientations are studied here, first modelled in Ansoft HFSS, and
then fabricated and measured. The three models are of the surface ripple running parallel to, at 45°
to, and perpendicular to the length of microstrip trace, as shown in Figure 4.1.

(i)   (ii)   (iii)
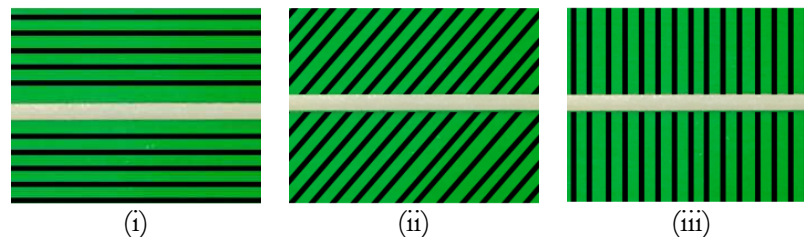
Figure 4.1 Surface ripple direction. (i) parallel to, (ii) at 45° to, and (iii) perpendicular to microstrip
trace direction.

The basic HFSS model is shown in Figure 4.2. The design consists of a 15 mm x 50 mm x
32 mil (thick) ABS substrate modelled with $\varepsilon_r = 2.58$ and $tan\delta = 0.0078$, and a 2.3 mm wide
CB028 trace with a conductivity of 1.65E6 S/m. The surface ripple model is only applied to the area
immediately surrounding the trace, rather than the entire substrate surface, to minimize the
complexity of the mesh. In each simulation, the height of the surface ripple (radius of the cylinder) is
swept up to 100 µm, in increments of 10 µm. In each case the height of the CB028 trace is 30 µm
above the peak of the ripple, which represents a reasonable approximation to actual printed line
heights. This is depicted graphically in Figure 4.3.
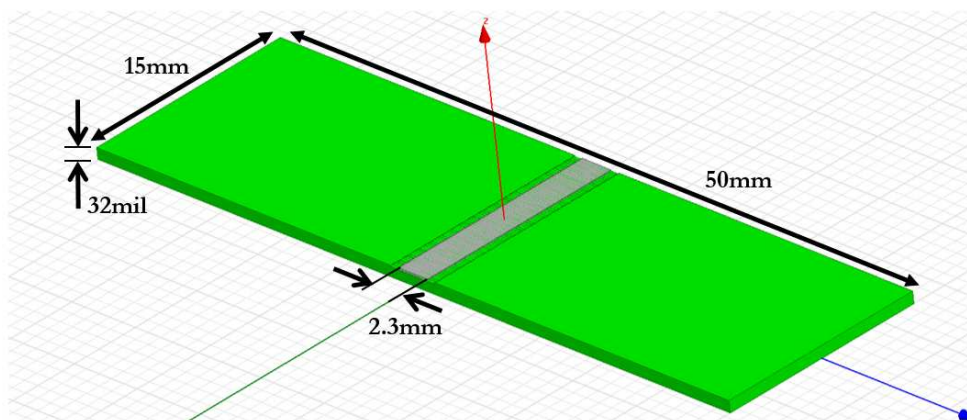
Figure 4.2 Basic HFSS model setup.
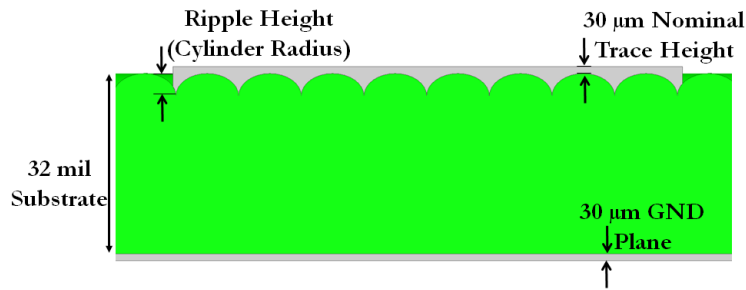
Figure 4.3 Basic HFSS model setup, cross section.

Figure 4.4 shows the HFSS model with surface ripples running parallel to the trace. Figure 4.5 shows the simulated S21 (dB) of the parallel ripple model, with the height of the ripple ranging from 30 μm to 100 μm. It is apparent from these plots that as the size of the ripples increase, the loss of the line increases.
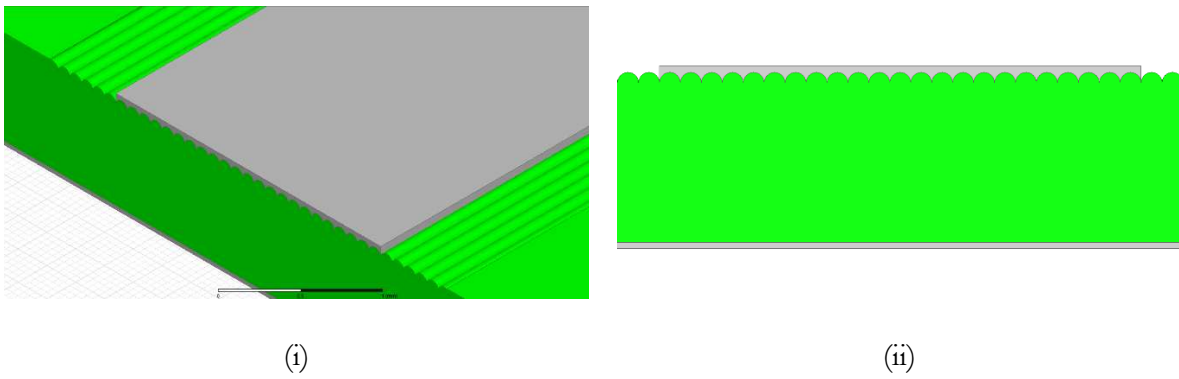
(i)   (ii)
Figure 4.4 Parallel surface ripple model. (i) Isometric view. (ii) Cross section.
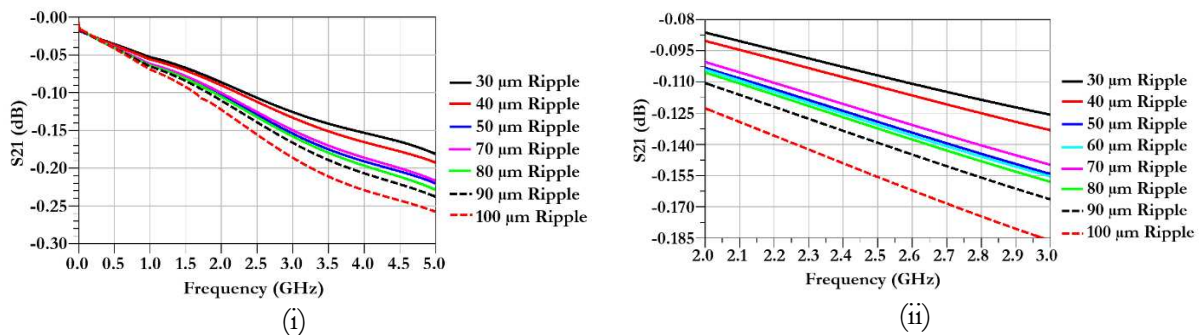
(i)   (ii)
Figure 4.5 S21 of 15mm 50Ω line with parallel surface ripple of varying heights. (i) 0-5 GHz. (ii) 2.0 – 3.0 GHz.

Figure 4.6 and Figure 4.7 show a cross section of the trace, at the edge and trace center, respectively, with the current density field plot shown over the geometry. The high current regions are in the valleys between the surface ripples. Since these ripples run parallel to the trace, this cross section is constant for the entire length of the trace. With this in mind, the proportional relationship between loss and ripple height makes intuitive sense. Reducing the ripple height results in a greater number of valleys per trace width. With a large ripple height, the current is confined to the narrowest parts of a small number of valleys due to the skin effect [18], increasing the effective resistance of the current path. As the ripple height decreases, the valleys become shallower and the current density occupies a greater cross-sectional conductor area. In the limit, as the ripple height approaches zero, the valley height is zero, and the surface becomes perfectly flat, which is an ideal condition.

(i) (ii)
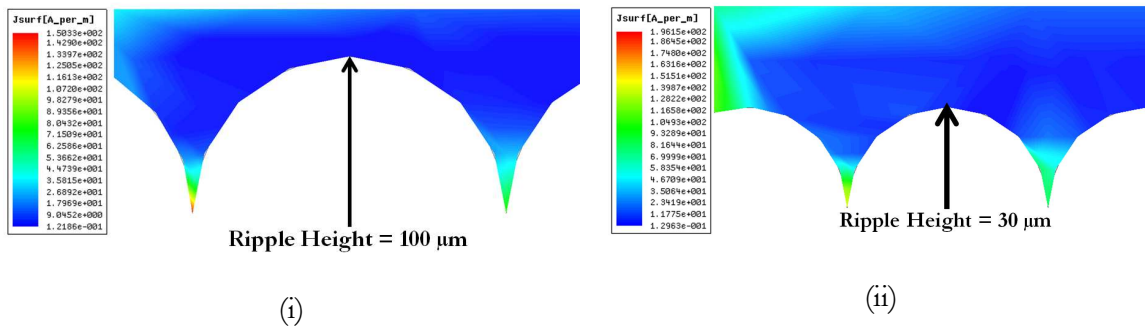
Figure 4.6 Trace cross section showing current density distribution at the edge of the trace with parallel surface ripple. (i) 100 μm ripple. (ii) 30 μm ripple.

(i) (ii)
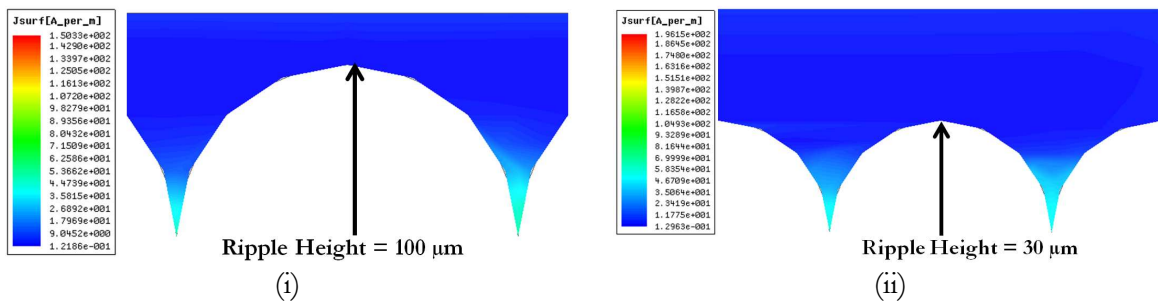
Figure 4.7 Trace cross section showing current density distribution at the center of the trace with parallel surface ripple. (i) 100 μm ripple (ii) 30 μm ripple.

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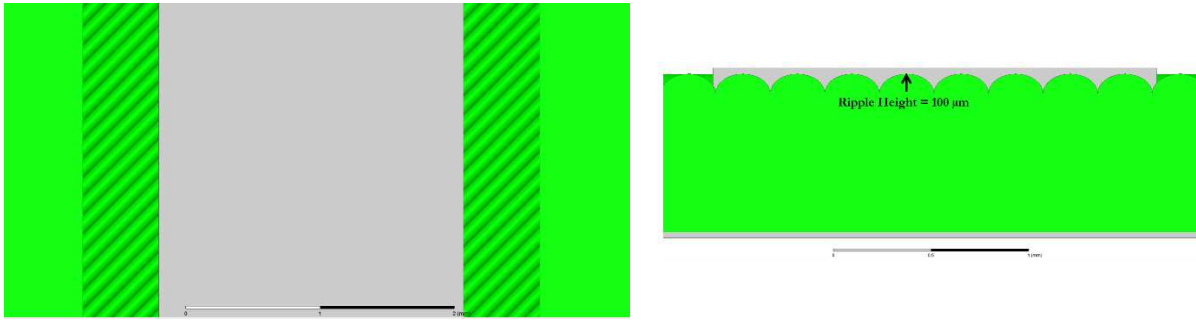
(i) (ii)

Figure 4.8 45° surface ripple model. (i) Top view. (ii) Cross section.
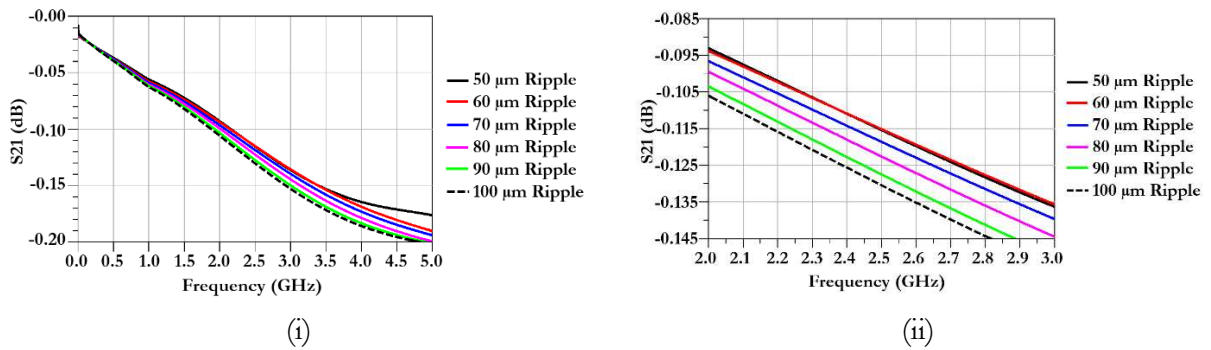
(i) (ii)

Figure 4.9 S21 of 15mm 50Ω line with 45° surface ripple of varying heights. (i) 0-5GHz. (ii) 2.0 – 3.0 GHz.
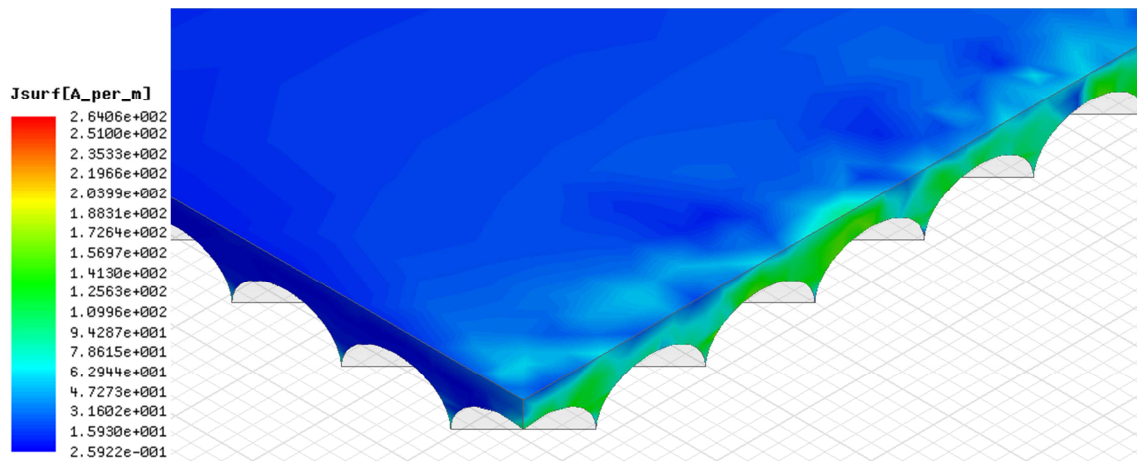
Figure 4.10 Isometric view of 45° surface ripple current density.

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Figure 4.8 shows the 45° ripple model and Figure 4.9 shows the simulated S21 (dB) with the height of the ripple ranging from 50 μm to 100 μm. Again, it is clear that loss increases with ripple height. Figure 4.10 shows an isometric view of the trace, with the current density field overlaid. The current distribution along the long edge is similar to that of the perpendicular ripple simulations, whereby the high current areas are at the peak of the ripples. Figure 4.11 shows the underside of the trace, again with the current density fields overlaid. 50 μm and 100 μm ripples are shown. Here there are high current density regions in every ripple valley, across the entire width of the trace. For the parallel ripple case, the geometry of the current path was constant over the length of the trace, but with the surface ripple rotated, this is no longer the case. The path now undulates, so the cross sectional area of the conductor oscillates, along the length of the trace, between its maxima and minima. Figures 4.10 and 4.11 show that the current conforms, to some extent, to the ripple, which effectively increases the length of the path seen by the energy. This could cause a negative frequency shift, as will be explained later in this section.

(i)   (ii)
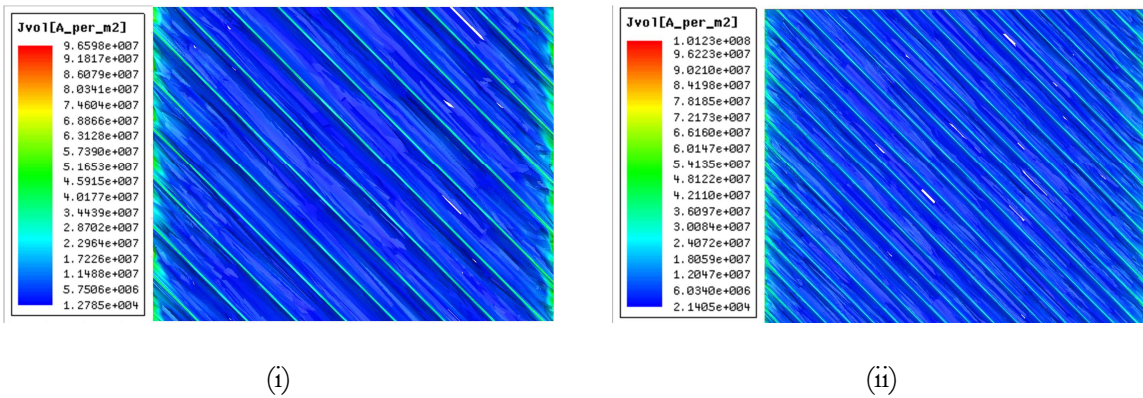
Figure 4.11 Current density of the 45° surface ripple simulation, viewed from below. (i) 100 μm ripple. (ii) 50 μm ripple.

Figure 4.12 shows the perpendicular ripple model and Figure 4.13 shows the simulated S21 (dB) with the height of the ripple ranging from 40 μm to 100 μm. Figure 4.14 and Figure 4.15 show the current distribution at the edge of the conductor, where once again it is seen that the current, to some extent, conforms to the ripple, and the maximum densities occur where the cross-sectional

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surface area is at its minimum. This is shown unequivocally in Figure 4.16 which shows the surface current vector field along the bottom of a section of the conductor. It is clear from this field plot and Figure 4.15 that the current only conforms to the undulations to some extent, because the current density in the lowest parts of the valleys is low.

<table>
<tr><td>(i)</td><td>(ii)</td></tr>
</table>
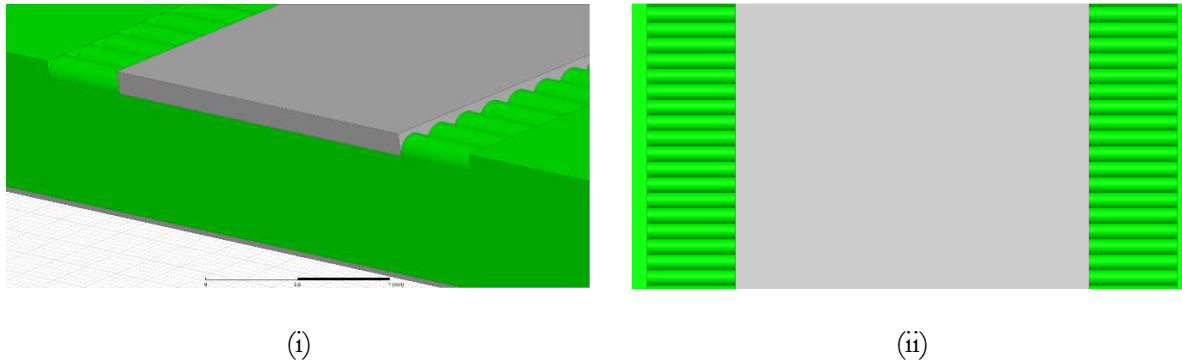
Figure 4.12 Perpendicular surface ripple model. (i) Isometric view. (ii) Top view.

<table>
<tr><td>(i)</td><td>(ii)</td></tr>
</table>
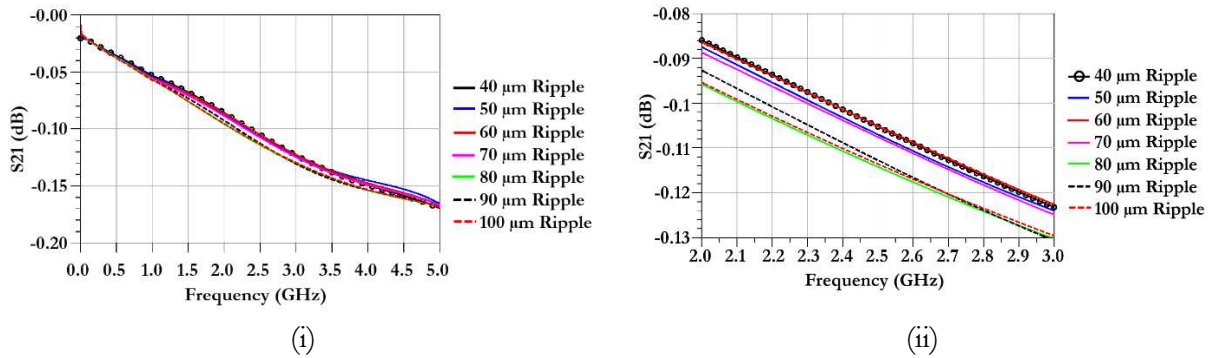
Figure 4.13 S21 of 15mm 50Ω line with perpendicular surface ripple of varying heights. (i) 0-5GHz. (ii) 2.0 – 3.0 GHz.

The current follows a wavy path, but does not follow the exact path of a series of adjacent semi-circles. As mentioned in the previous paragraph, this behavior may lead to a negative frequency shift. A worst case scenario of this effect can be shown mathematically with some assumptions. If it is assumed that all of the current precisely follows the contours on the bottom of the trace, as depicted in Figure 4.17, then over the linear distance of a trace designed to be of length λ, the current follows a path of length $\lambda_l = \frac{\pi}{2}\lambda$. From this, the change in frequency from the design

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frequency, f_{Design}, to the frequency corrected for the extension of the current path, $f_{Corrected}$, can be calculated as:

$$\frac{f_{Corrected}}{f_{Design}} = \frac{c/\lambda_I}{c/\lambda} = \frac{\lambda}{\lambda_I} = \frac{2}{\pi} \tag{4.1}$$

so,

$$f_{Corrected} = \frac{2}{\pi} f_{Design} \tag{4.2}$$

which shows that, in the worst case, the design frequency may be reduced to 64% of its intended value, in the presence of this surface ripple. This effect will never be so pronounced in practice, since the current does not perfectly follow the semi-circular path, and not all current flows along the bottom surface, however it is an important factor to consider.
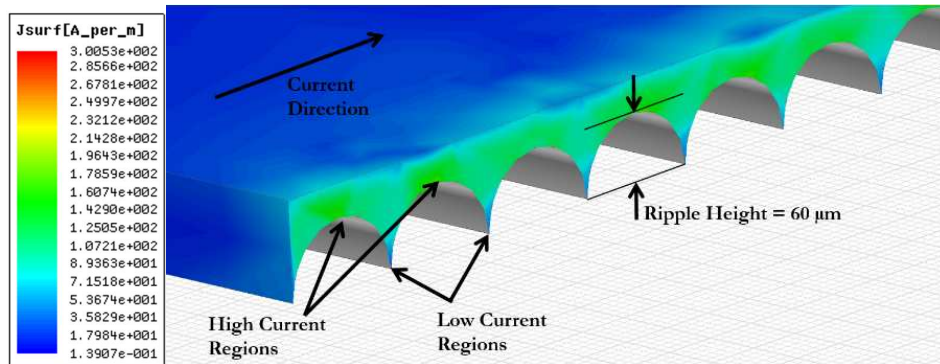
Figure 4.14 Isometric view of trace with perpendicular ripple showing current distribution.
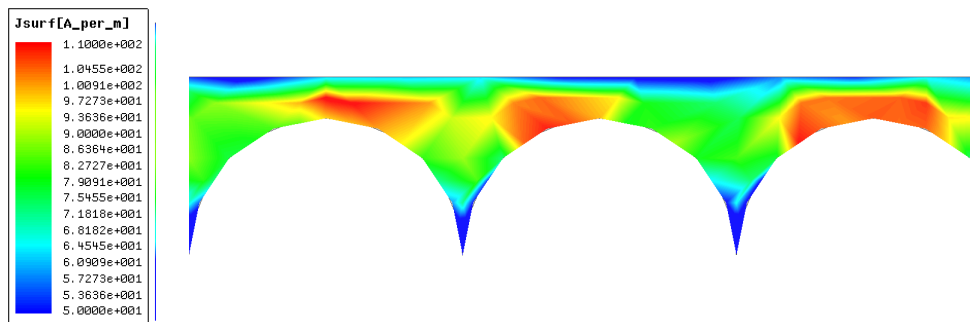
Figure 4.15 Surface current density along the edge of the trace with a perpendicular surface ripple of 50 µm height.
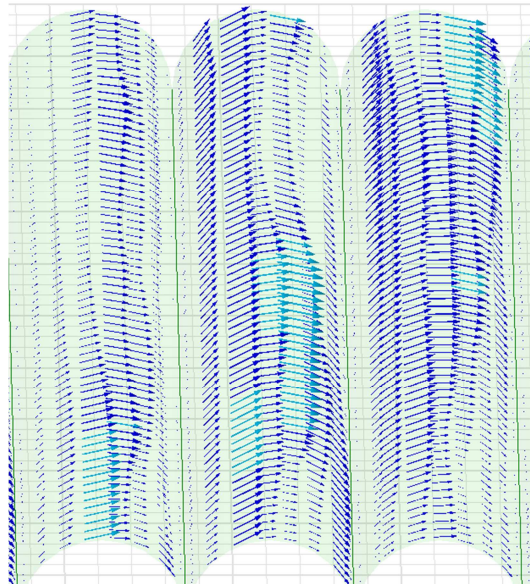
Figure 4.16 Surface current vector field along bottom surface of conductor.
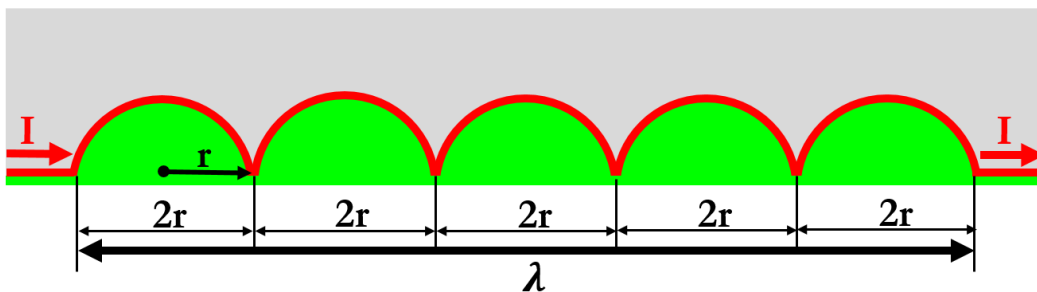
Figure 4.17 Ideal model of worst case current path over a rippled substrate.

When considering the feasibility of materials for electronics packaging, it is important to consider the thermal response of the materials. To this end, HFSS and Ansoft steady state thermal simulations are performed using a large microstrip section. Using Ansoft Workbench as a hub, HFSS is used to model the electrical performance of a structure. The surface loss density and volume loss density of the model are then exported, via Workbench, into the steady state thermal simulation, which calculates the temperatures in the structure due to heat generated from the electrical losses. In HFSS, it is common to evaluate conductors on the surface only, since the skin depth effect makes this simplification reasonable for high conductivity materials. In this case, the

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surface loss density of the conductor is used for the thermal load due to the ohmic losses in the conductors, and the volume loss density is used for the thermal load due to the dielectric losses in the substrate. However, since CB028 is being modelled with a conductivity of 1.65E6 S/m, at 2.45 GHz the skin depth is 7.9 μm, which is around 6 times deeper than copper. For this reason, the CB028 traces are evaluated over the entire volume.
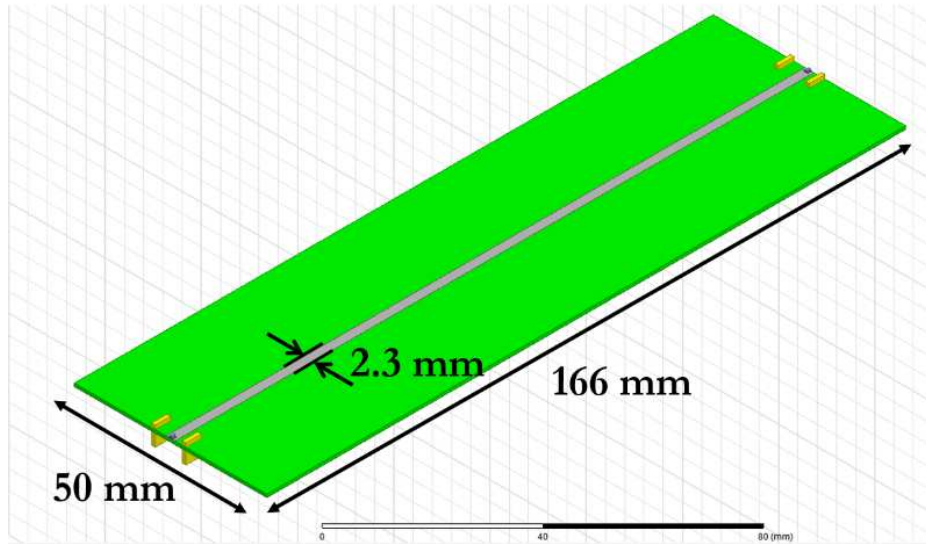
Figure 4.18 HFSS model for thermal simulations.

For these simulations, perfect dielectric surfaces are used, rather than the rippled surface of the previous section. The thermal conductivity of CB028 is not known, and although the thermal conductivity of ABS is known to be in the range of 0.17 – 0.19 W/(mK) [19], it is assumed that the thermal conductivity of *printed* ABS is lower, due to the potential inclusion of air pockets in the bulk printed material. The thermal conductivity of CB028 and ABS is assumed, for the purposes of these simulations, to be 20 W/(mK), and 0.16 W/(mK), respectively. For H20E the data sheet value of 29 W/mK was used. The actual CB028 value is not known, so it is simply assumed to be lower than that of H20E by an arbitrary 9 W/mK. The only material parameter required for steady state thermal simulations is thermal conductivity. The model used for the HFSS portion of these simulations is shown in Figure 4.18. The thermal simulation includes a convection boundary applied

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to every external face of the model. Stagnant air has a convection coefficient of 5 W/(m² °C), according to the software preset. Once again, a value for this variable was assumed. It is unlikely that the air in the lab would be perfectly stagnant, so a value of 10 W/(m² °C) was used. This value was used in [20]and [21], with the former justifying the value experimentally in a lab environment. The simulations are sensitive to this parameter, but the results obtained are reasonable. The result of the thermal simulation is shown in Figure 4.19.
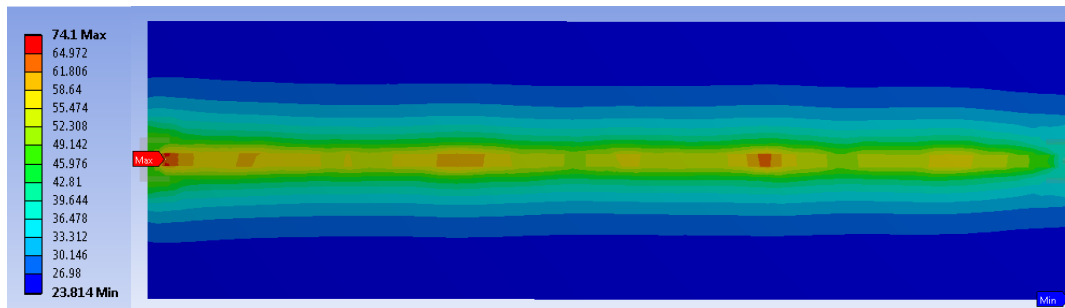
Figure 4.19 Thermal simulation results of microstrip section with an RF input power of 41 dBm.

4.3 Microstrip Fabrication

Having simulated the electrical and thermal responses of microstrip lines fabricated using DDM techniques, an analysis of the performance of fabricated microstrip lines follows. For the purposes of comparison, a similar microstrip line fabricated using traditional techniques is also fabricated. This microstrip line is fabricated on a Rogers 4003C microwave laminate with a 32 mil substrate. This board, along with three DDM microstrip lines with parallel, 45°, and perpendicular surface ripples are shown in Figure 4.20. Figure 4.21 shows S21 and S11 of the four samples. These measurements demonstrate that the DDM fabricated sample with surface ripples running parallel to the trace has the lowest insertion loss, which is contrary to the simulations. These values, though, differ by only tenths of a dB, so there are likely other real-world factors influencing the results, such as the epoxy connections to the connector pins, and non-uniformity in the microstrip and substrate dimensions. Figure 4.22 shows photographs of the three DDM lines at 4X magnification. This

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shows the non-uniformity of the trace dimensions. The width of the trace varies with the ripple in the ABS surface.
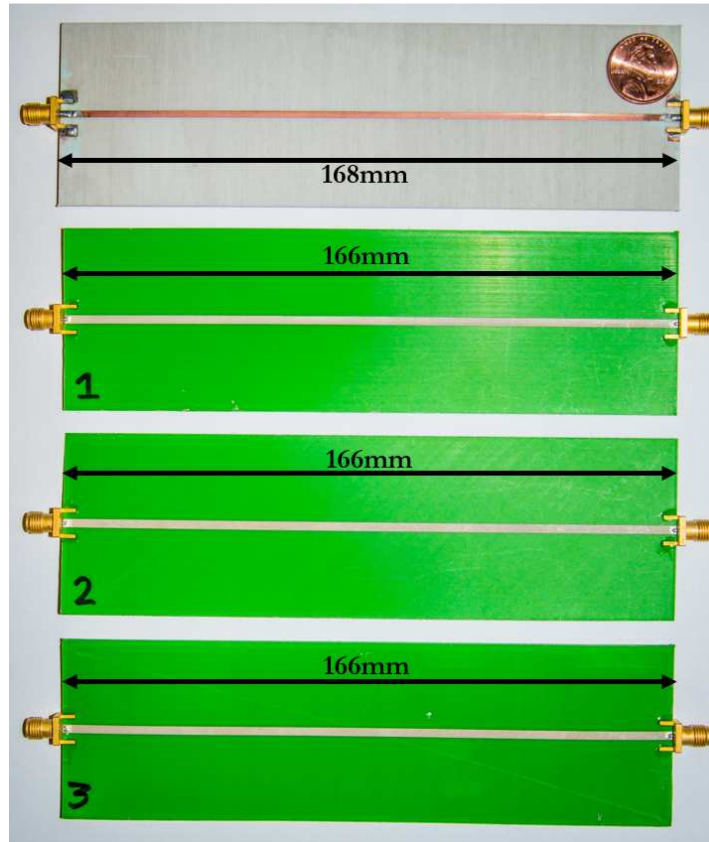
Figure 4.20 Fabricated microstrip samples. Rogers 4003C and DDM versions with parallel, 45°, and perpendicular surface ripples.
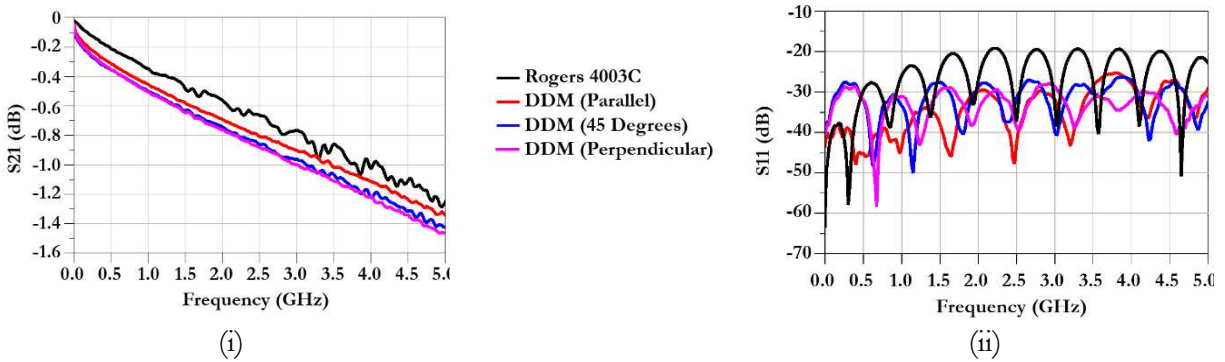
Figure 4.21 S21 (i) and S11 (ii) of the four fabricated microstrip samples.
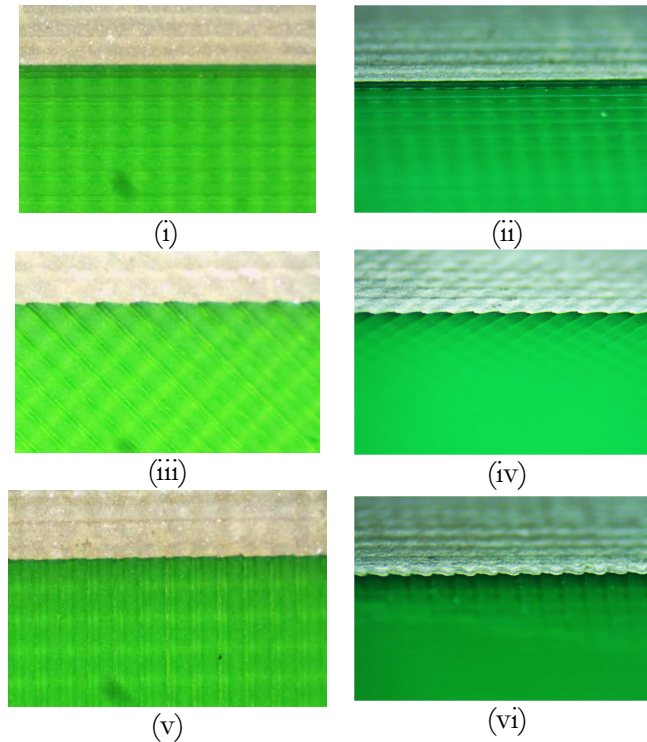
Figure 4.22 Photos of the DDM fabricated microstrip samples at 4X magnification. (i) Parallel ripple, top view. (ii) Parallel ripple, side view. (iii) 45° ripple, top view. (iv) 45° ripple, side view. (v) Perpendicular ripple, top view. (vi) Perpendicular ripple, side view.

Figure 4.23 shows cross-section profilometer measurements of the perpendicular ripple sample. Here, it is apparent that ripple not only exists in the ABS surface, but also in the CB028 surface. This CB028 surface ripple is not a result of the filling in of the ABS ripple, but rather an artifact of the ink printing process, which draws the outline of the trace, then fills in the center with a back-and-forth motion. This is evident when comparing the CB028 profile of other samples, and noting that the CB028 ripple does not in any way correspond to the ABS ripple. Figure 4.24 shows similar measurements of the 45° ripple sample. Here it is more evident that the ABS surface is not particularly cylindrical, and the width is about eight times the height. Figure 4.25 shows the trace cross section of the parallel ripple simple, and the profile along the length of the trace. This shows the relative non-uniformity of the trace height, with a maximum deviation of around 2µm.
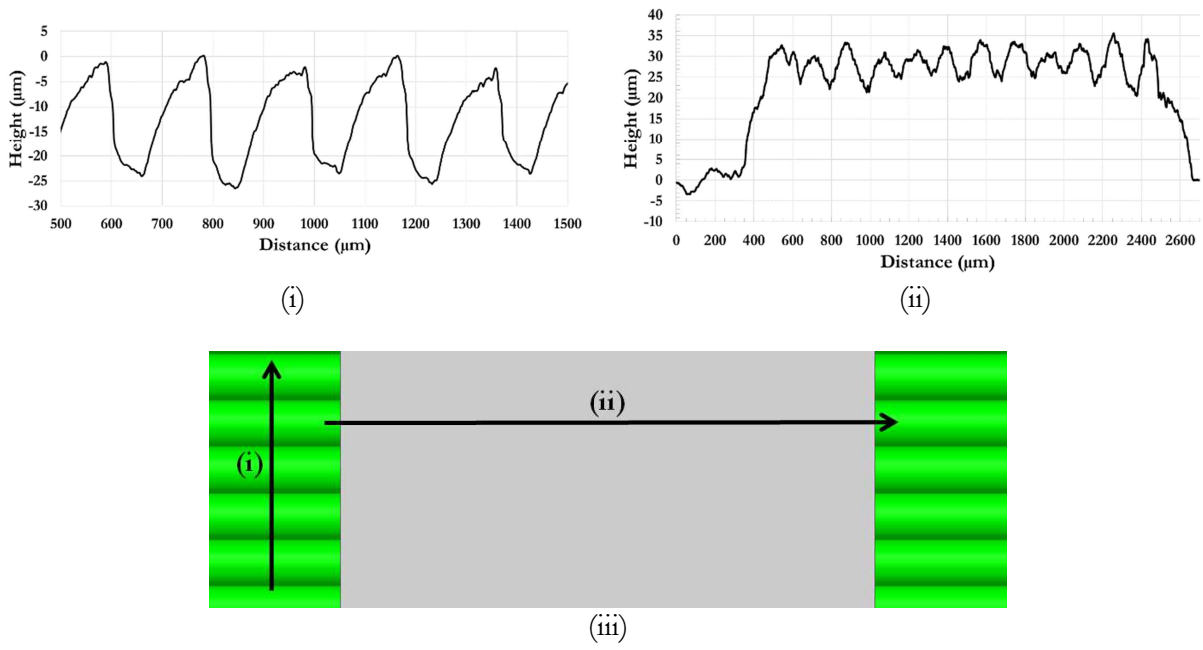
Figure 4.23 Profilometer measurements of the perpendicular surface ripple sample. (i) ABS cross section. (ii) Trace cross section. (iii) Profilometer scan directions.
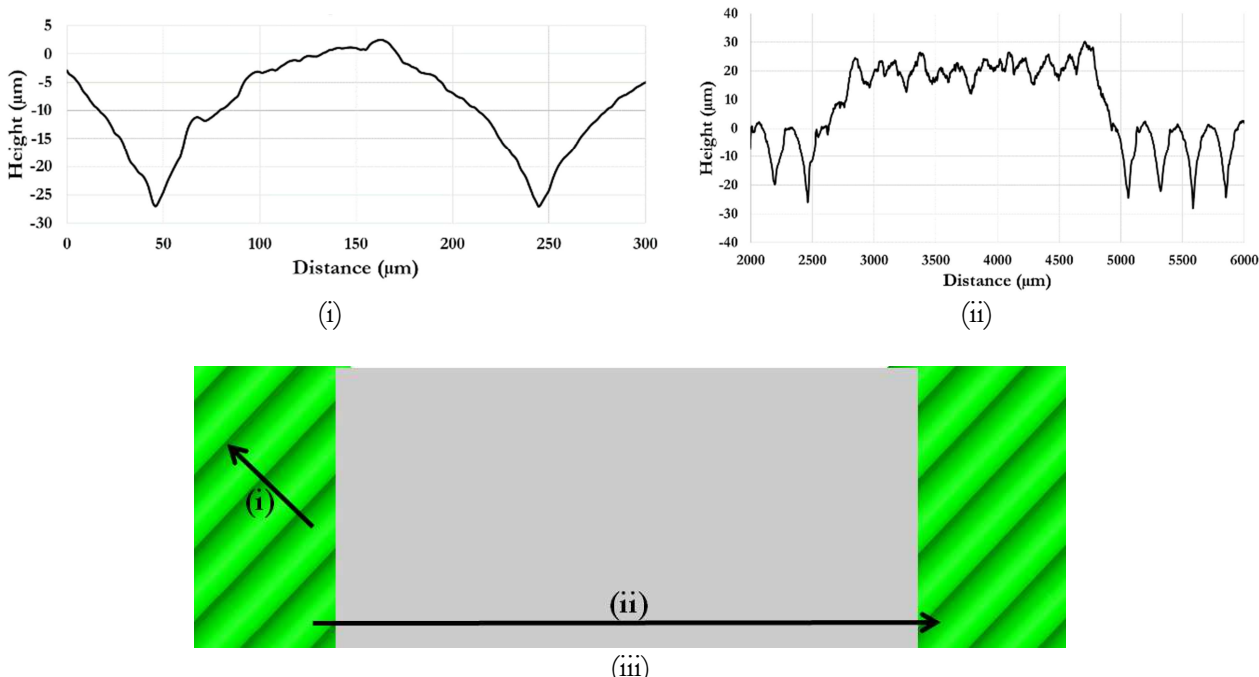
Figure 4.24 Profilometer measurements of the 45° surface ripple sample. (i) ABS cross section. (ii) Trace cross section. (iii) Profilometer scan directions.
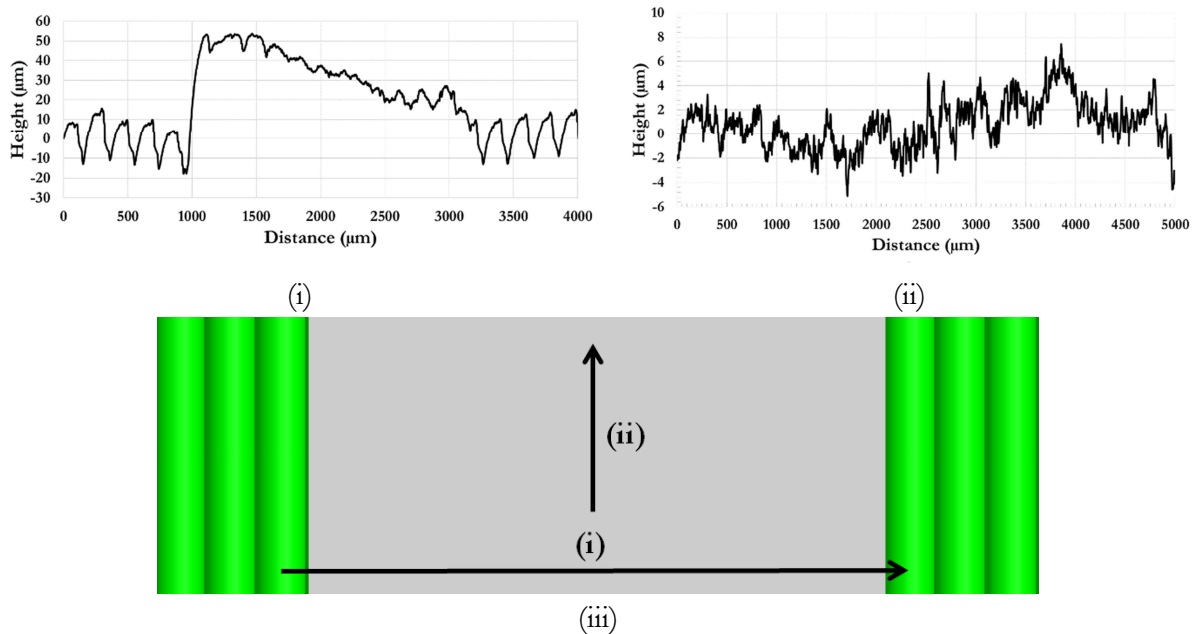
Figure 4.25 Profilometer measurements of the parallel surface ripple section. (i) Trace & ABS cross section. (ii) Along the length of the trace. (iii) Profilometer scan directions.

To test the power handling capability and the thermal response of a DDM fabricated microstrip, the instrumentation setup depicted in Figure 4.26 is used. This setup primarily uses a signal generator, an amplifier, and a spectrum analyzer to apply a 2.45 GHz signal of increasing power to the microstrip sample (DUT), and measure the power at the output. Due to the fact that large signals are being utilized here, there is around 43 dB of attenuation after the DUT. The insertion losses of the system components were measured independently, and their values are calibrated out of the measurements so that true input and output powers of the DUT could be assessed. The goal of these measurements is to verify that the materials of these DDM fabricated transmission lines operate linearly over a series of power inputs, and that the temperatures achieved are sustainable over time. A Keysight TrueIR U5855A thermal camera was used for all temperature measurements and thermal images. It is also important to verify the re-usability of these devices, so the measurements are repeated five times, with 41 dBm RF power applied to the DUT for 30 minutes in between each measurement. The results of these measurements are shown in Figure 4.27.

These plots show a rapid rise in maximum temperature after 35 dBm RF input power. The maximum temperature on the line was measured to be 74°C with 41 dBm input to the microstrip line. This temperature is approaching the glass transition temperature of ABS, so operation above this point at this frequency would likely begin to deteriorate in performance. Figure 4.27(ii) shows the results of the five rounds of power cycling. The response for all five is practically identical, which is a satisfactory result as it demonstrates that the materials can support relatively high power throughputs repeatedly, without degradation of performance.
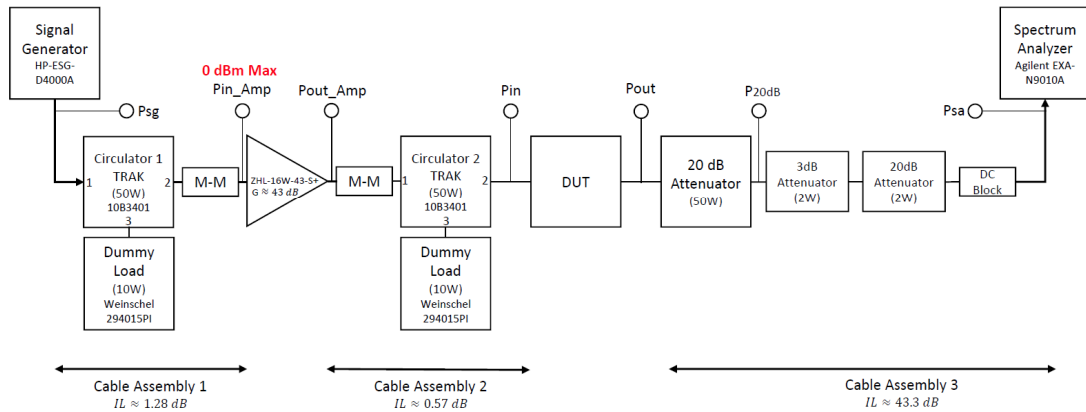
Figure 4.26 Block diagram of the power handling measurements setup.

| (i) | (ii) |
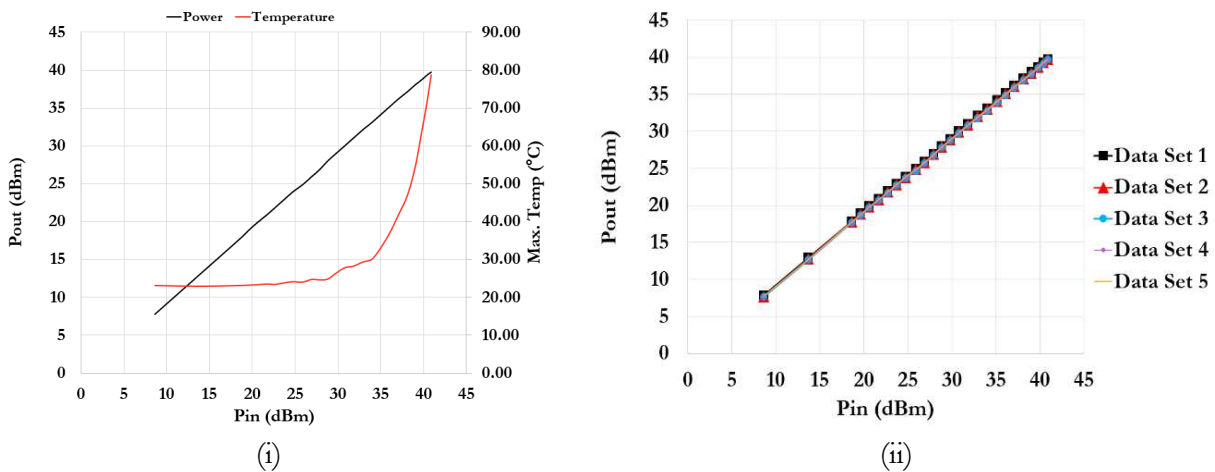
Figure 4.27 Power handling and thermal response of DDM 166mm 50Ω microstrip line. (i) Power vs Temperature. (ii) Pout vs Pin, with 41 dBm of RF power applied for 30 minutes between each data set.

Figure 4.28 shows the thermal response of the microstrip line with 41 dBm RF power applied. The maximum steady state temperature on the line is 74°C. The S11 plot of Figure 4.21 shows that the lines are all well matched at 2.45 GHz. The temperature plot along profile line 1, which runs along the center of the trace, shows a temperature gradient from input to output, as expected. For a perfectly matched line, though, where there is no standing wave present on the line, it is expected that this curve would resemble an exponential decay curve [22]. Figure 4.28 does not represent a perfect exponential decay in temperature, indicating that there is standing wave on the line, which of course indicates some mismatch. A standing wave results in high and low voltage/current regions, which result in high/low temperature spots. Figure 4.28(i) has clear "hot spots" around pixels 140, 1990, and 240, which are equally spaced, as expected.
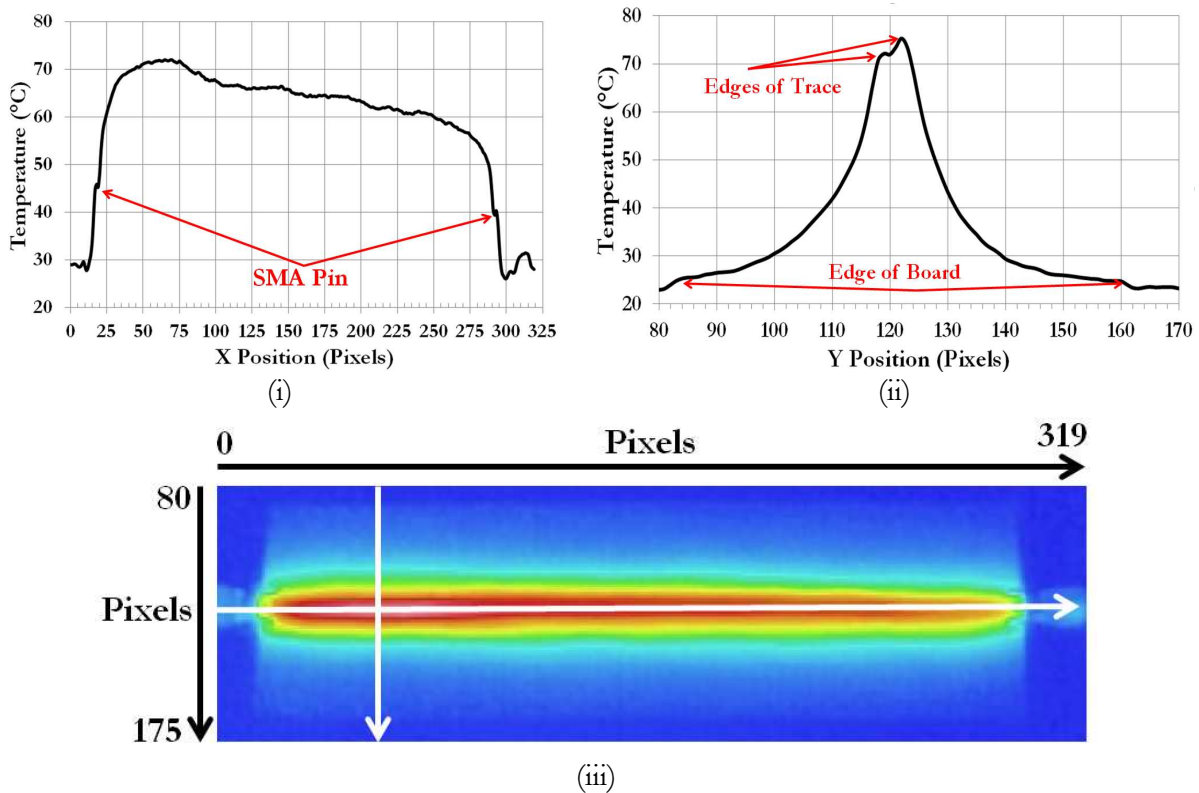
Figure 4.28 Thermal measurements of 166mm 50Ω microstrip line. (i) Temperature profile along "Profile Line 1." (ii) Temperature profile along "Profile Line 2." (iii) Thermal image of a microstrip sample.

Comparing this measured result with the simulation of Figure 4.19, there is some minor discrepancy, but the temperature ranges are reasonable. The fabricated line width of the parallel ripple microstrip line is 2.19 mm, not 2.3 mm as simulated. Another thermal simulation with a line width of 2.19 mm and all other parameters left as given above yields a slightly better agreement, as shown in Figure 4.29. Here the range of temperatures displayed is well matched, and the temperature profile of the line is also in good agreement. The location of the maximum temperature is shifted slightly towards the input, but this location is related to the amount of heat dissipated by the connector. The connector model is dimensionally accurate, but it is unlikely to be a functionally perfect representation of the actual connector.
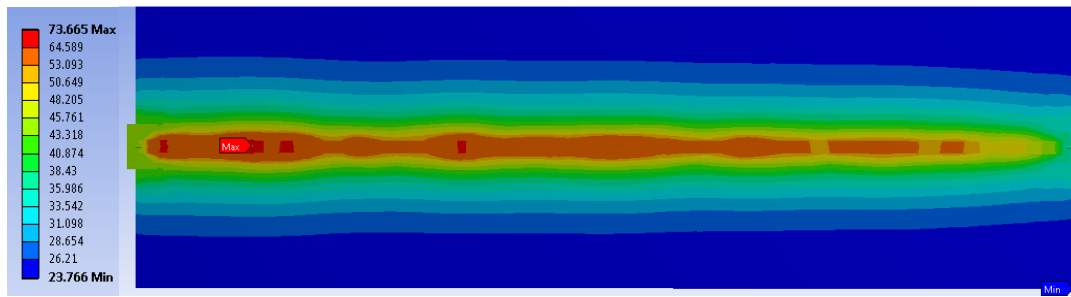
Figure 4.29 Thermal simulation with modified trace width.

Table 4.1, 4.2, and 4.3 compare the simulated and measured loss per meter for the three ABS ripple configurations. In this plot, return loss is ignored, since it is below 30dB in every case. These results are plotted in Figure 4.30. This plot demonstrates the proportional relationship between ripple height and normalized loss, for each configuration.

4.4 Conclusion

This chapter has demonstrated that DDM technology and materials are capable of producing microwave devices with predictable electrical and thermal performance. One of the criteria given in Chapter 3 for determining the suitability of a packaging was the ability to produce

transmission lines of desired characteristic impedance. This capability has certainly been demonstrated.

The materials used here exhibit relatively high loss compared to copper and various popular dielectric substrates, which is potentially problematic in itself. Further to that, though, is the increase in temperature that results may pose further problems for some applications. Many microwave devices are thermally sensitive, so this may preclude the use of this technology in some specific applications. While the microstrip lines presented here performed as expected at 41 dBm at 2.45 GHz, it would not be recommended to operate them at higher powers than this. The low thermal conductivity of the materials may also be problematic when dealing with active devices that have thermal management issues. This issue is investigated in Chapter 5.

The work in this chapter was assigned a clearance of CLEARED on October 8, 2015 (Case Number: 88ABW-2015-4858).

Table 4.1 Comparison of microstrip performance with perpendicular surface ripple.

$f_c = 2.45GHz$	Insertion Loss (dB)	dB/m
Measured (~25 μm ripple)	0.871	5.3
40 μm Ripple	0.103	6.9
50 μm Ripple	0.105	7.0
60 μm Ripple	0.103	6.9
70 μm Ripple	0.106	7.1
80 μm Ripple	0.112	7.5
90 μm Ripple	0.111	7.4
100 μm Ripple	0.112	7.5

Table 4.2 Comparison of microstrip performance with 45° surface ripple.

$f_c = 2.45GHz$	Insertion Loss (dB)	dB/m
Measured (~25 μm ripple)	0.842	5.1
50 μm Ripple	0.113	7.5
60 μm Ripple	0.113	7.8
70 μm Ripple	0.116	7.7
80 μm Ripple	0.120	8
90 μm Ripple	0.125	8.3
100 μm Ripple	0.128	8.5

Table 4.3 Comparison of microstrip performance with parallel surface ripple.

$Fc = 2.45GHz$	Insertion Loss (dB)	dB / m
Measured (~25 μm ripple)	0.788	4.7
30 μm Ripple	0.105	7
30 μm Ripple	0.11	7.3
50 μm Ripple	0.127	8.5
60 μm Ripple	0.128	8.5
70 μm Ripple	0.123	8.2
80 μm Ripple	0.13	8.7
90 μm Ripple	0.136	9.1
100 μm Ripple	0.152	10.1

Figure 4.30 Loss vs surface ripple height of simulated and measured microstrip lines with three ABS ripple configurations.

CHAPTER 5: IC INTEGRATION

5.1 Introduction

In this chapter, DDM techniques are used to fabricate printed circuit boards (PCB) for IC devices. The study of electronics packaging technologies would not be complete without an investigation into the ability to embed IC devices into the structure, given the ubiquitous nature of such electronic devices at this point in time.

There are some important challenges at hand. ABS is a low temperature material with a glass transition temperature of 100°C-110°C, so it is not possible to solder components to the traces. That aside, DuPont does not recommend soldering to CB028 conductive traces. The thermal concerns do not end with the inability to use solder. Active devices are never 100% efficient, and power amplifiers can reach temperatures that surpass the glass transition temperature of ABS. In traditional PCB manufacturing, high thermal conductivity materials such as copper are used, so thermal management tends to be handled, in the simplest case, with well-placed vias and a ground plane. For the DDM approach studied in this thesis, the thermal conductivities of compatible materials are very low, compared to copper. H20E, a conductive epoxy, is used for thermal management issues in industry at present, but its thermal conductivity is only 29 W/mK [23] while copper is 401 W/mK [24]. H20E must be cured above 80°C, so its own thermal requirements are ideal for this application. H20E is used here to bond IC devices to the PCB, and for the thermal management approach presented here.

In this chapter, two IC devices with different package types are investigated. The first is an RF switch with lead style connections, and the second is an RF front end with pad style connections.

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The lead style connections are relatively simple to connect to a board using epoxy, but the pad style connections are problematic due to the paste-like state of the epoxy. These pads work well when soldering, since molten solder naturally flows to the heated metal, and hardens instantaneously. This is not so for epoxy, which takes several hours at 80°C to harden, and can spread out beneath the package with minimal applied pressure. The RF front end device includes a low noise amplifier (LNA) and a power amplifier (PA) which has thermal management requirements. The package contains a large (with respect to the area of the chip) metal pad on the bottom of the chip, which is to be used for thermal management, so the board layout design must include a means to address this issue.

Section 5.2 discusses the fabrication of the RF switch board, and compares simulated results to measured results. The measurement results from two DDM fabricated boards are presented, as well as a traditionally produced Rogers 4003C board, and the performance is compared.

Section 5.3 discusses the fabrication of the RF front end board, and a first attempt at handling the thermal management requirements of the device. Measurement data for the LNA and PA are presented, as well as thermal analysis and power handling for each.

5.2 RF Switch

A Macom MASWSS0115 GaAs SPDT switch with an operating frequency range of DC – 3.0 GHz is integrated into a DDM fabricated test board. The board uses a 32 mil ABS substrate, and all conductive traces are printed with DuPont CB028. A similar board fabricated on 32 mil Rogers 4003C is also designed so that the performance of the two fabrication technologies may be compared. Figure 5.1 shows a schematic layout of the board design, a photograph of the Rogers 4003C fabricated board, and a photograph of the DDM fabricated board.

For this particular device, the manufacturer provides a set of S-parameters for each output path. Using this data, the DDM fabricated version is simulated using Keysight Advanced Design

www.manaraa.com

System and Momentum. The layout performance is simulated in Momentum. Modelithics ATC 600S full parasitic capacitor models, and the above mentioned S-parameters for the switch are then combined with the Momentum data to form a full device simulation. For the purposes of simulation, the conductivity of CB028 is 9E5 S/m, $\epsilon_{r,ABS} = 2.58$, and $tan\delta_{ABS} = 0.0078$.

(i)

(ii)

(iii)
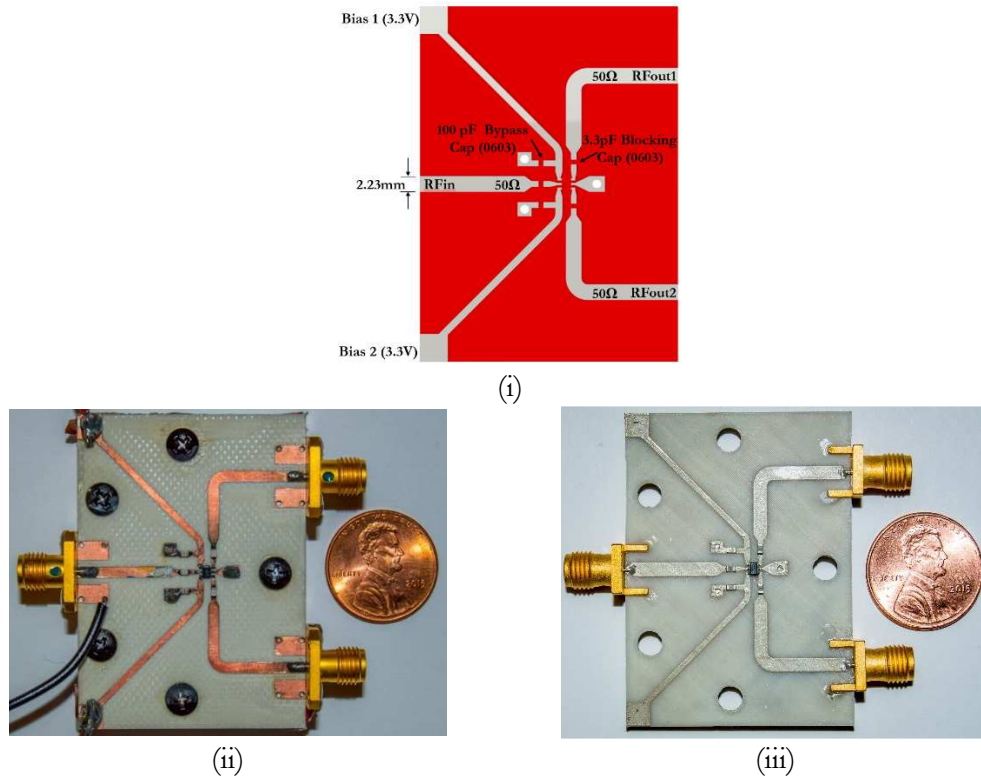
Figure 5.1 MASWSS0115 RF switch board. (i) Board layout. (ii) Photo of fabricated and populated Rogers 4003C board. (iii) Photo of DDM fabricated and populated board.

Figure 5.2 shows the S-parameters of a first version of the DDM fabricated board, with 4.7pF blocking capacitors. The blocking capacitor values have significant effect on the frequency placement of the resonance. As the capacitor value increases, the resonance frequency decreases. The data sheet recommends a 39pF capacitor at 2.45 GHz, but this value caused a resonance at only 600MHz, leaving an unacceptable return loss and 2.45 GHz. A 4.7 pF capacitor yielded a resonance at around 2.1 GHz. Figure 5.2 compares the simulated and measured results with this blocking capacitor, with both RF1 and RF2 enabled, alternately. There is relatively close agreement between

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simulations and measured data, however the measured results are slightly negative frequency shifted. This negative frequency shift is predicted in Chapter 4, and so can at least partially be attributed to the 45° surface ripple present on these boards. Another cause is perhaps that the PCB used by the manufacturer to generate the S-parameters was coplanar waveguide, not microstrip. While the supplied S-parameters are de-embedded to the device pins, it is possible that this difference in structure causes some discrepancy, also.

Table 5.1 and Table 5.2 show the pertinent numerical data for each plot shown. Here, S21 and S12 have the same value. These values, though, vary by 0.1dB with respect to RF1 and RF2 being enabled. This difference is not present in simulation, and it is indeed an unexpected result. One would expect the insertion loss to be the same, regardless of which path is enabled. This difference is likely due to the assembly of the board. The H20E was applied to the pins and capacitors manually, so it is certainly not done uniformly. This is also true of the connectors.
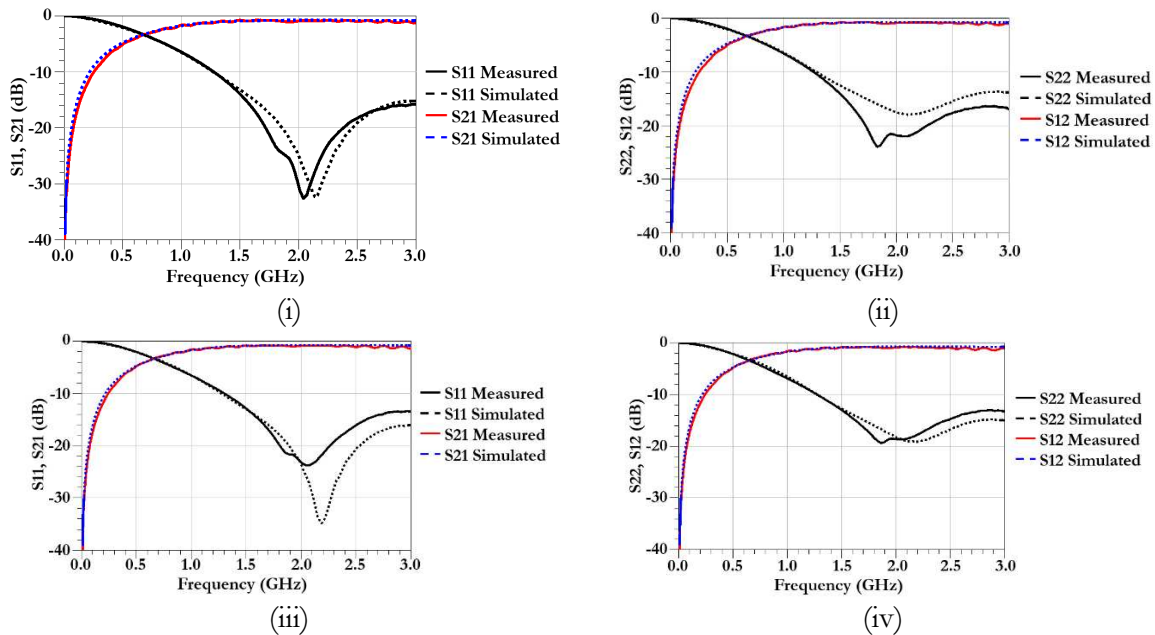
Figure 5.2 S-parameters for the first DDM fabricated switch board, with 4.7pF blocking capacitors. (i) & (ii) RF1 enabled. (iii) & (iv) RF2 enabled.

Figure 5.3 shows the measured S-parameters of the Rogers 4003C switch board using 3.9pF blocking capacitors. The results are in close agreement with the data-sheet values. There is, as expected, a small amount of extra loss, given that the data sheet data is de-embedded to the device pins. There is some discrepancy between S12 and S21 with both RF1 and RF2 enabled, which is assumed to be a small measurement error.
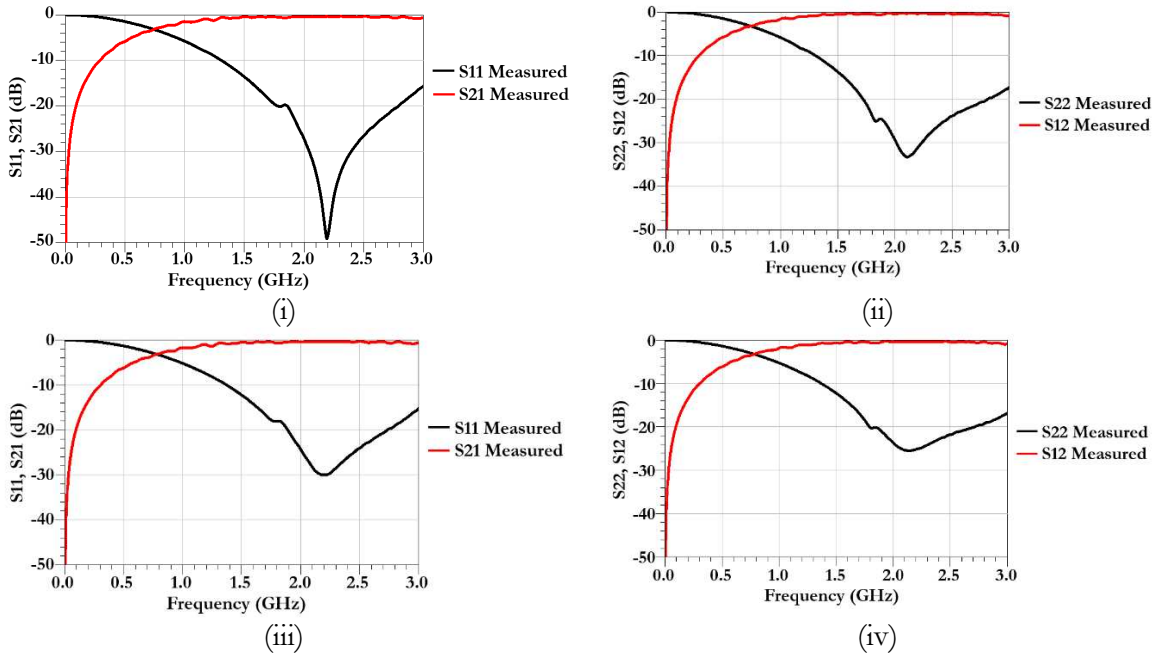
Figure 5.3 S-parameters for the Rogers 4003C switch board, with 3.9pF blocking capacitors. (i) & (ii) RF1 enabled. (iii) & (iv) RF2 enabled.

Figure 5.4 shows the measured S-parameters of the second DDM fabricated board with 3.9 pF blocking capacitors. The plots compare measured and simulated data. Once again, there is a negative frequency shift in the measured data, which is more pronounced in RF2 than RF1. The insertion loss is extremely high in this fabrication, compared to the simulated data. It is, of course, expected that the insertion loss of the DDM fabricated version is worse than the Rogers 4003C version, but these results are much worse than expected. The RF2 path is better than the RF1 path. Comparing these results to the first DDM print, with the 4.7pF blocking capacitors, it is clear that there is something other than the change of capacitance value present in these results. The first print

showed a reasonable insertion loss, while the second does not, even with an improved return loss at 2.45 GHz. The manual nature of the assembly of these devices, and the variation of quality between various prints leads to the potential for non-uniform results. To be truly scientific in the characterization of these DDM fabricated devices, a repeatable process must be present at all stages of production. The least reproducible aspect of these fabrications is the manual assembly of the boards, and the attachment to a 3D printed carrier. To be reproducible, an automated pick and place machine should be used to place the components on the board, and the SmartPump™ should be used do dispense small dots of H20E, which it is more than capable of doing.
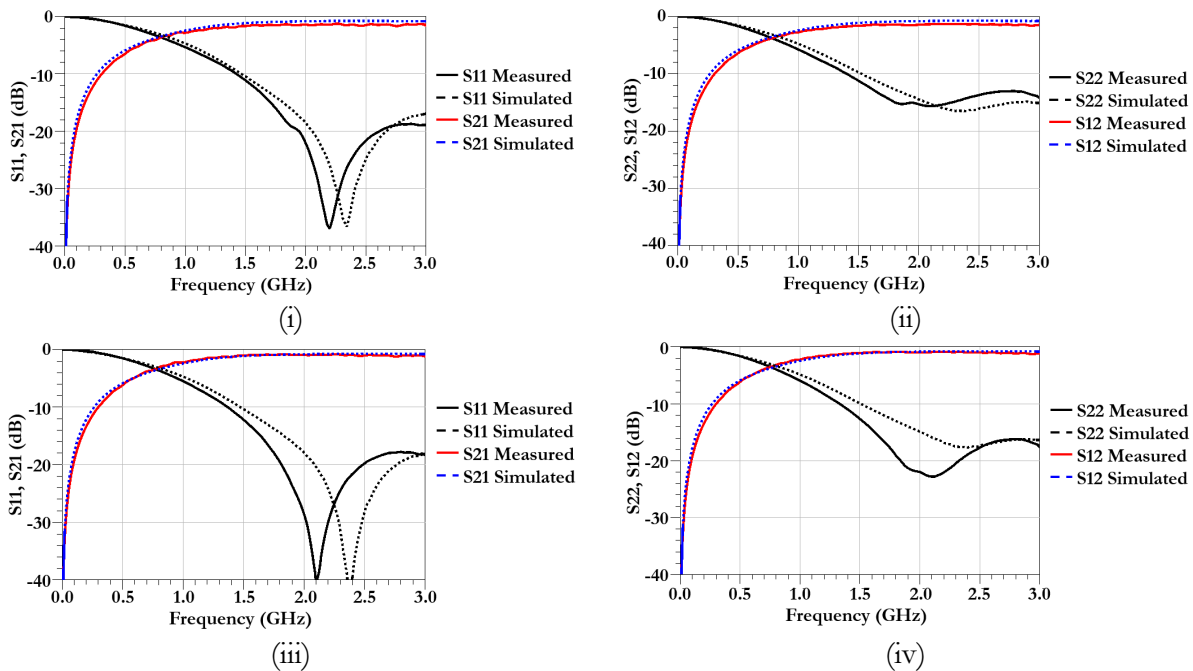
Figure 5.4 S-parameters for the DDM fabricated switch board, with 3.9pF blocking capacitors. (i) & (ii) RF1 enabled. (iii) & (iv) RF2 enabled.

Figure 5.5 shows a comparison of S-parameters between the DDM fabricated board, and the Rogers 4003C board. There is good agreement between the performances of each fabrication methods, albeit with significantly worse insertion loss in the DDM fabricated version, as discussed above. It is believed that this insertion loss issue is not emblematic of poor material performance in the ABS or CB028, rather an issue with assembly. It is also possible, in retrospect, that the epoxy

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connections were not sufficiently cured, which would indeed result in a lower conductivity of the epoxy, and thus decreased insertion loss performance.
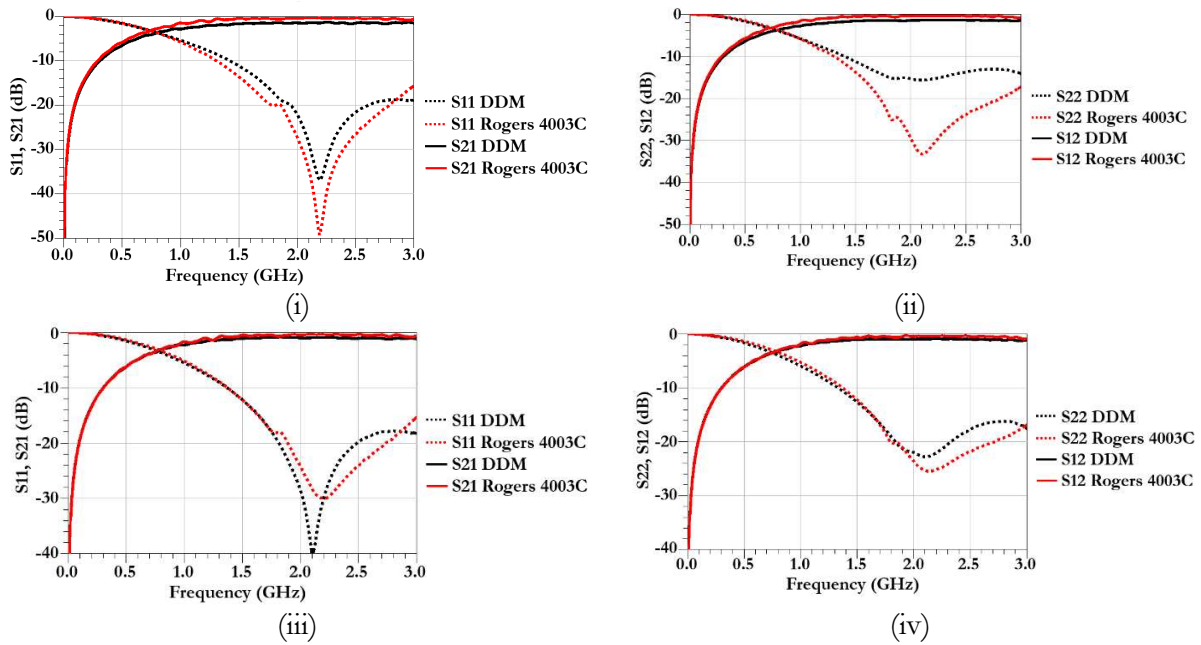
Figure 5.5 S-parameters for the DDM fabricated switch board compared to the Rogers, with 3.9pF blocking capacitors. (i) & (ii) RF1 enabled. (iii) & (iv) RF2 enabled.

Finally, Figure 5.6 shows the power handling performance of the DDM fabricated switch board. The materials maintain linearity, and input 1dB compression of the switch is around 28dBm, in accordance with that given in the data sheet.
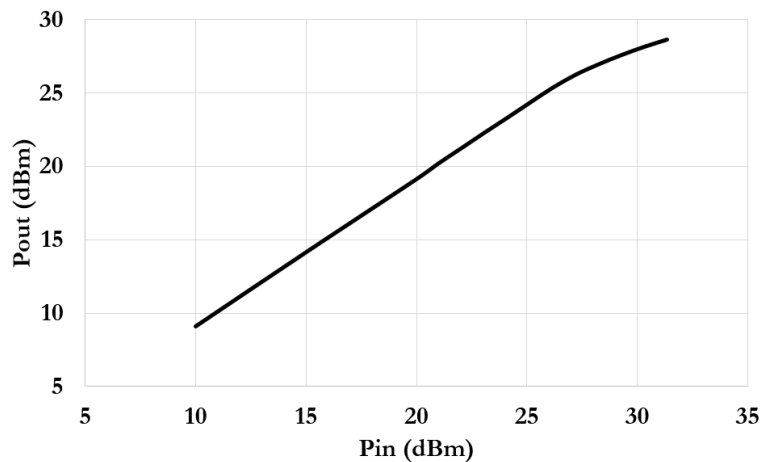
Figure 5.6 Power analysis of the RF switch. P_{in} vs P_{out}.

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Table 5.1 Switch measurement data at 2.45 GHz (RF1 enabled). Rogers 4003C and DDM compared.

| f_c=2.45GHz | \|S11\| | | | \|S21\| | | | \|S12\| | | | \|S22\| | |
	(dB)	>10 dB Bandwidth (%)	(dB)	+ 0.2 dB Bandwidth (%)	(dB)	+ 0.2 dB Bandwidth (%)	(dB)	>10 dB Bandwidth (%)
DDM (4.7 pF, Measured)	18.8	70.2	0.9	29.8	0.9	44.9	18.0	70.6
DDM (4.7 pF, Simulated)	20.7	58.0	0.8	53.5	0.8	53.5	16.3	61.2
Rogers 4003C (3.9pF, Measured)	28.1	69.0	0.5	53.9	0.38	73.1	24.8	68.7
DDM (3.9 pF, Measured)	22.7	64.1	1.7	64.1	1.4	39.6	14.0	65.3
DDM (3.9 pF, Simulated)	27.5	62.4	0.8	53.5	0.8	53.1	16.3	60.0

Table 5.2 Switch measurement data at 2.45 GHz (RF2 enabled). Rogers 4003C and DDM compared.

| f_c=2.45GHz | \|S11\| | | | \|S21\| | | | \|S12\| | | | \|S22\| | |
	(dB)	>10 dB Bandwidth (%)	(dB)	+ 0.2 dB Bandwidth (%)	(dB)	+ 0.2 dB Bandwidth (%)	(dB)	>10 dB Bandwidth (%)
DDM (4.7 pF, Measured)	16.8	69.4	1.0	56.3	1.0	46.5	15.12	70.2
DDM (4.7 pF, Simulated)	22.7	62.4	0.8	54.3	0.8	53.5	15.8	60
Rogers 4003C (3.9pF, Measured)	25.1	66.5	0.5	58.4	0.4	38.0	22.4	66.5
DDM (3.9 pF, Measured)	20.6	66.5	1.1	65.0	1.0	55.1	18.3	68.2
DDM (3.9 pF, Simulated)	32.4	62.4	0.8	56.0	0.8	53.5	17.5	60

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5.3 PA/LNA

A single 2.45 GHz RF front end IC device is integrated into a DDM fabricated test board. The IC device used is the Skyworks SE2613T, which includes a low noise amplifier for receive mode and a power amplifier for transmit mode. The maximum output power of the power amplifier given by the data sheet is 31dBm. It has been demonstrated in Chapter 3 that ABS/CB028 fabrications are more than capable of supporting this power level. The question remains, though, as to whether or not the materials can support the heat generated by an amplifier, concentrated to a small region. The SE2613T uses a UQFN-16 package, whose dimensions are 3mm x 3mm x 0.6mm. The pads are 0.25mm wide, and spaced 0.5mm apart. Figure 5.7 shows the layout and dimensions of the package. One particular area of concern is the large ground pad at the bottom of the device. The purpose of this is to pull heat away from the device, so that it may be dissipated through some PCB embedded thermal management design. Due to the low-temperature nature of the fabrication materials, components cannot be soldered to the boards. Instead, H20E, a conductive epoxy is used. H20E is used commercially for thermal management [23], as it has a relatively high thermal conductivity. This property is exploited in this board design.
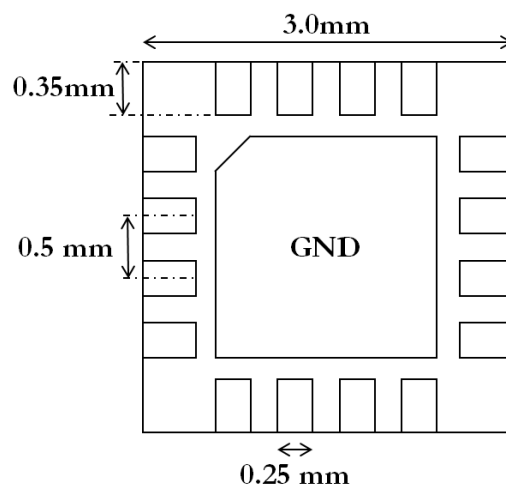
Figure 5.7 UQFN-16 package layout and dimensions.

Figure 5.8 shows the layout of the test board design, and a photograph of the fabricated and populated board. Wires for DC biasing are epoxied to the board, a shown.
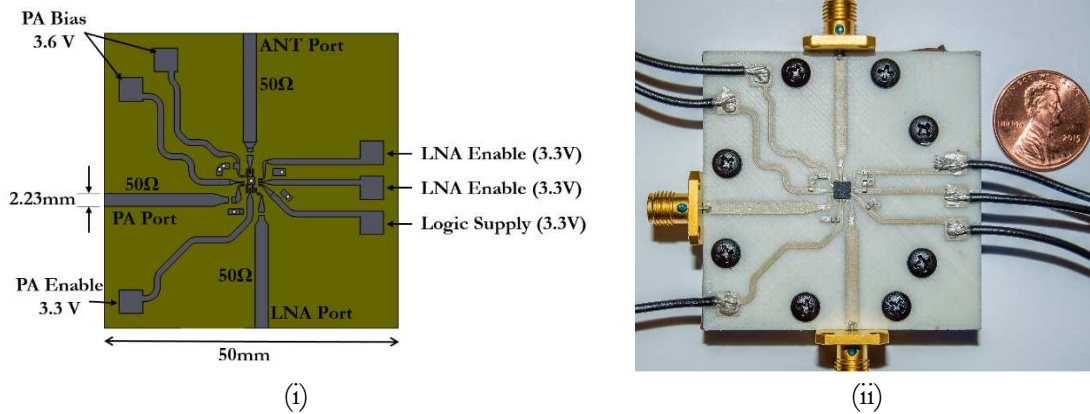
Figure 5.8 (i) SE2613 2.45GHz RF Front end board layout and (ii) photo of fabricated and populated board.

Figure 5.9 shows photographs of the epoxy connections to the IC package, an 0603 capacitor package, and the SMA connector's pin. A significant drawback in the technology at present is the lack of automation. These component connections are made by hand, which is not ideal when dealing with such small dimensions. The IC package has pads which are designed for bonding on the underside of the package. Given the manual nature of this process, however, epoxy is only applied to the 0.15mm tall section of pad that appears on the side walls of the package. It is likely that performance is affected due to this as the pads are made wider with epoxy, leaving a smaller gap between pads, and only a small connection area is made.

Figure 5.10 shows the method employed for thermal management. A single via hole of 0.6mm diameter is included in the ABS substrate print, and a pad of CB028 is printed surrounding it. The walls of the via hole are coated with CB028. Prior to placing the chip, the via hole is filled with H20E which, as mentioned earlier, has a relatively high thermal conductivity. Once cured, the chip is then bonded, again using H20E, to the CB028 pad. In theory, this provides a low resistivity

path to ground, due to the skin effect, for the signal, and a high thermal conductivity path for the heat generated by the chip.
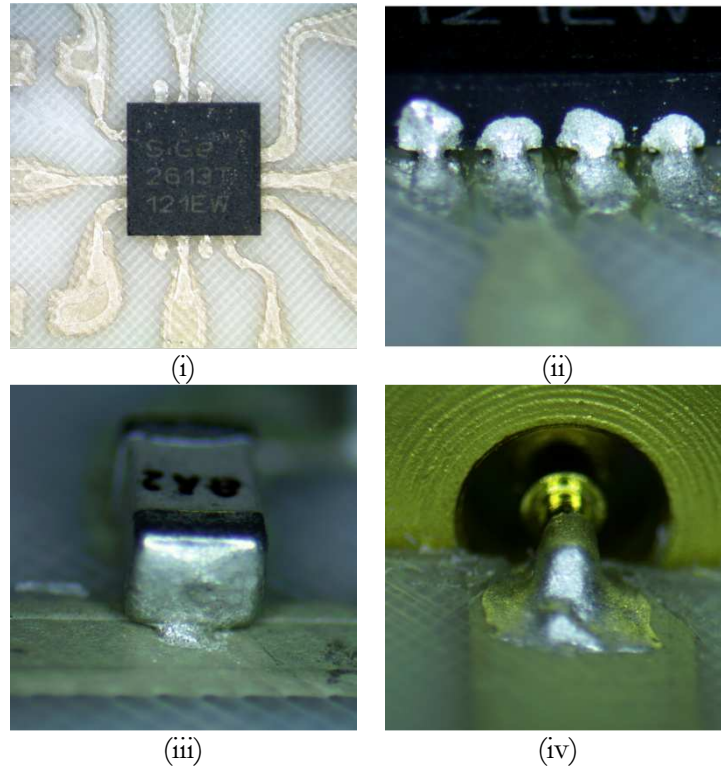
Figure 5.9 SE2613T board photos. (i) SE2613T placed, top view. (ii) SE2613T epoxy connections. (iii) Epoxied capacitor. (iv) SMA connector epoxy connection.
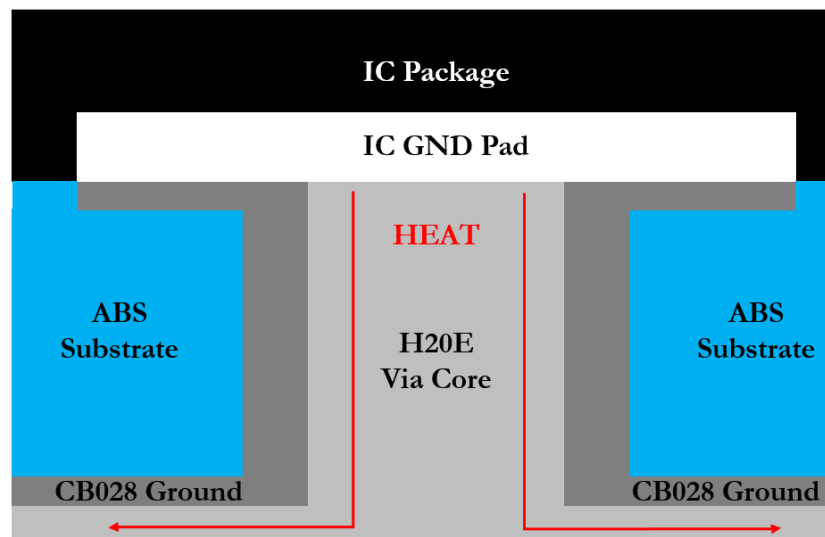
Figure 5.10 Cross section of thermal management via concept.

Figure 5.11 shows the small signal S-parameters of the LNA and the PA. The pertinent values at 2.45 GHz are given in Table 5.3 and Table 5.4. The performance of the LNA is very close to being within specification. The data sheet specification values are de-embedded to the device pins, whereas the measured data is not, since this thesis is concerned with the effects of the package. The gain of the LNA is 10.2dB, which is just below the minimum data sheet gain of 11dB. Since the transmission lines are quite lossy, a reduction in gain is expected. The noise figure of the LNA was measured, using the Y-Factor method, as 2.46dB, which is 0.6dB above the data sheet specified value. As demonstrated in section 3.2, an increase in the noise figure is expected for lossy and mismatched transmission lines. If it is assumed that the transmission lines are perfect 50 Ω lines, then the noise figure of a lossy line is equal to its loss factor. This increase in noise figure, then, is consistent with the reduced gain, as described above.

(i)   (ii)
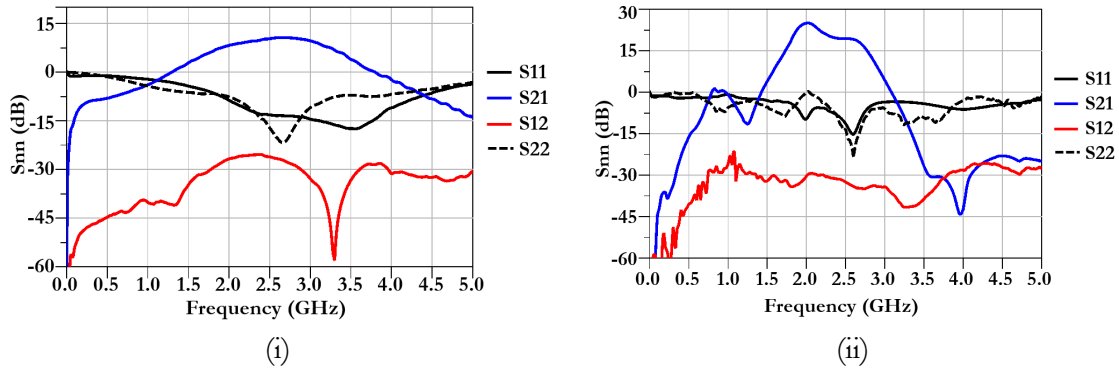
Figure 5.11 S-Parameter measurements of the SE2613T board. (i) Low noise amplifier (ii) Power amplifier

Table 5.3 LNA measurement and data sheet specifications compared.

f_c=2.45GHz	Data Sheet	Measured
Input Return Loss (dB)	10	13.4
Gain (dB)	Min. = 11, Typ. = 13, Max. = 15	10.2
Output Return Loss (dB)	10	21.5
Noise Figure (dB)	1.8	2.46
IP1dB	Min. = -6, Typ. = -5	>-5

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Table 5.4 PA measurement and data sheet specifications compared.

f_c=2.45GHz	Data Sheet	Measured
Input Return Loss (dB)	Typ. = 12, Max. = 10	9.7
Small Signal Gain (dB)	26	19.4

The PA does not perform as well as the LNA. The plot of Figure 5.11 shows some questionable behavior. The output return loss at 2.0 GHz is just above 0dB, which is indicative of oscillation. There is some uncertainty in the measurement here, though, due to a 20 dB attenuator at the output. To further investigate the possible oscillation, a 50 Ω load is connected to the PA input, and the output is viewed on a spectrum analyzer. There is no measurable signal produced with no applied input. The gain of the PA is measured as 19.4 dB, which is 6.6 dB below the gain specified in the device data sheet. It is possible that these oddities are a result of a poor ground connection beneath the device.

Figure 5.12 shows plots of output power and temperature vs. input power for the LNA and the PA, at the data sheet recommended bias points. There are two sets of data displayed here. The second set of data represents measurements made after operating the PA at almost full power (P_{in}=3.8dBm) for 30 minutes. The importance of this is apparent when considering Figure 5.14, which shows a thermal image and the temperature profile along a line under these conditions. The maximum temperature of the chip is around 160°C, which is well above the glass transition temperature of ABS. The fact that the device continued to operate, and produced the same response after being subjected to these temperatures for 30 minutes is indicative that the thermal management approach was at least partially valid. It appears, according to Figure 5.14 (ii) that the ABS is not heated above 105°C under these conditions. Figure 5.13 shows the thermal response of the LNA at maximum power.

The thermal response of the PA can be improved by reducing the PA bias voltage. This, of course, reduces the 1dB compression point, but this may not be of concern, depending on the application. Figure 5.15 shows plots of output power and temperature vs. input power with the power amplifier biased at 3.3V instead of 3.6V. It is clear that the device is beginning to compress slightly earlier than in Figure 5.12, but the temperature with 3dBm RF input power is reduced from around 160°C to around 123°C, which is a significant improvement. Under this configuration, the efficiency of the device improved. Further reductions in bias voltage were attempted, but below around 3.0V, the bias current begins to be supplemented by the logic power supply, so this is not considered a good operating condition.
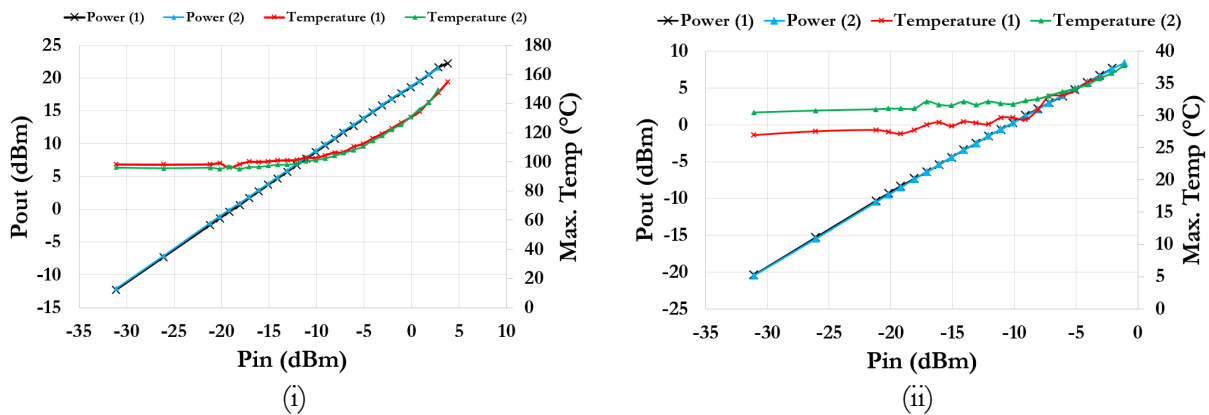
Figure 5.12 P_{out} & Temperature vs P_{in} of PA and LNA. (i) PA enabled.(ii) LNA enabled.
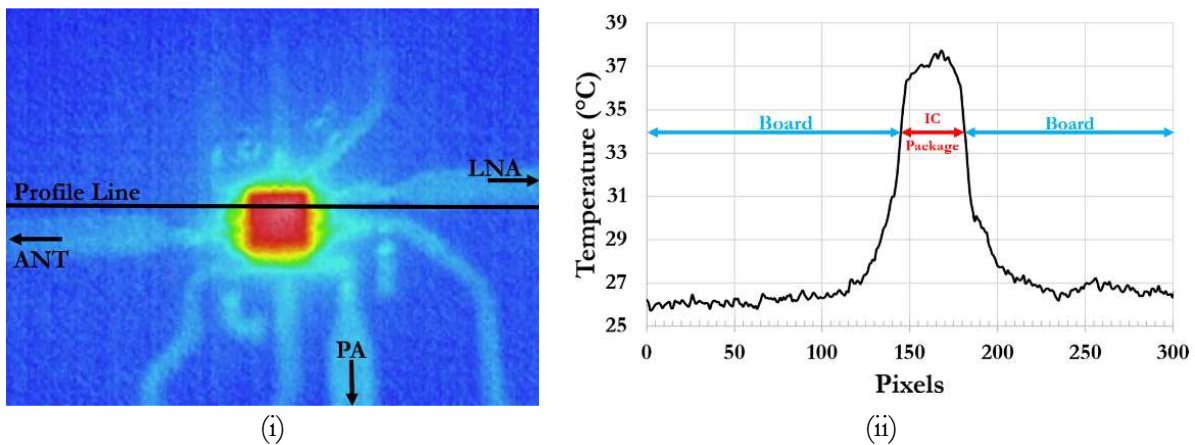
Figure 5.13 Temperature measurements with LNA enabled. (i) Thermal image, max input power. (ii) Temperature profile along "Profile Line."

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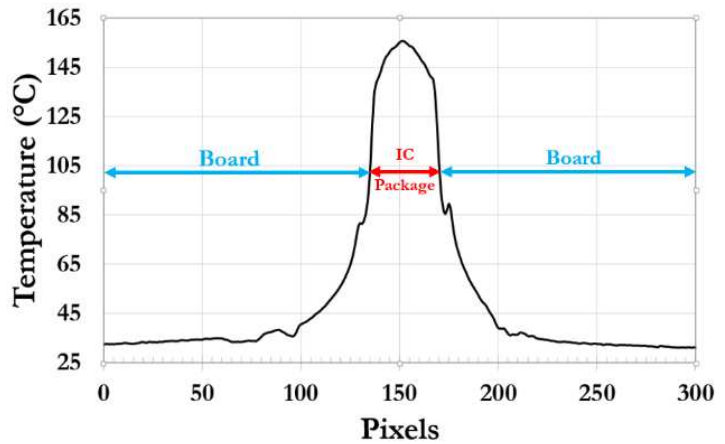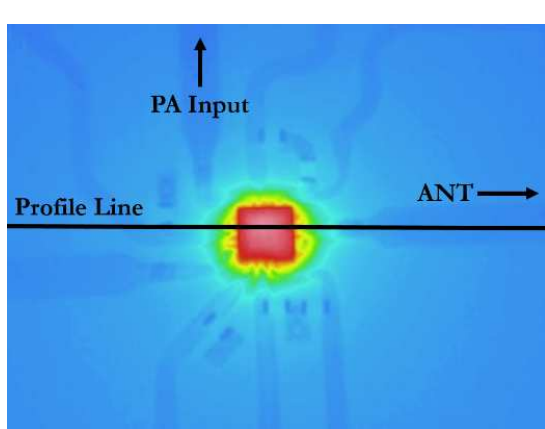
(i)   (ii)

Figure 5.14 Temperature measurements with PA enabled. (i) Thermal image, max input power. (ii) Temperature profile along "Profile Line."
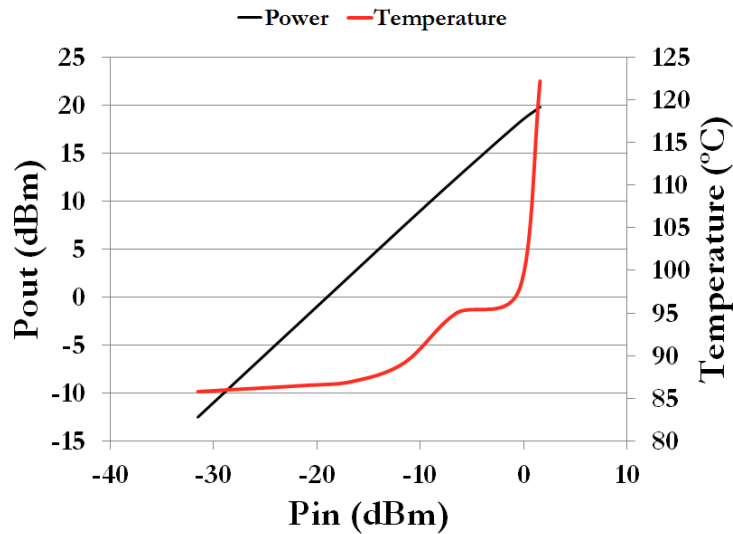
Figure 5.15 P_{out} & Temperature vs P_{in} of power amplifier, biased at 3.3V.

5.4 Conclusion

Through measurements of an RF switch and RF front end chip connected to DDM fabricated board, it is certain that this technology and these materials are viable for real-world RF applications. The technology is not perfect at present, as there are still some processes that must be completed by hand, which leads to an inevitable non-repeatability. The major missing feature is a pick-and-place, which would be used to automatically place IC devices, resistors, capacitors, etc., in

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their respective positions on a board. Combining the pick-and-place with nScrypt's SmartPump™ technology for precision epoxy dot placement would likely yield better and more repeatable results.

A potential short-coming of the approach is the H20E. While this epoxy has good thermal and electrical performance, it does have a propensity to crack with minimal applied pressure. Figure 5.16 shows an example of this, whereby the pin of an SMA connector is bonded to a trace using the epoxy. This crack occurred whilst screwing on an SMA cable for a measurement.

The work in this chapter was assigned a clearance of CLEARED on October 8, 2015 (Case Number: 88ABW-2015-4858).
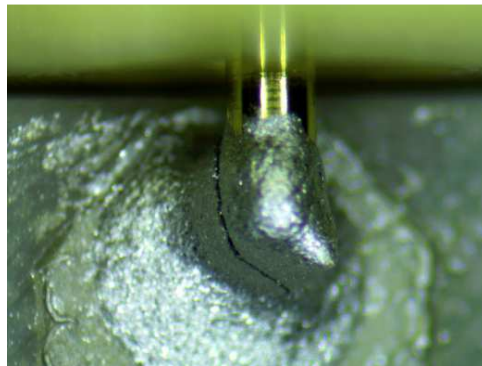
Figure 5.16 Cracked epoxy on SMA connector pin.

CHAPTER 6: DDM FABRICATED WILKINSON POWER DIVIDER

6.1 Introduction

The Wilkinson power divider has become a staple of microwave engineering. It can be found in many systems, including phased array antennas [25] and power amplifiers [26]. The purpose of this chapter is to present a 2.45 GHz 4-way equal split miniaturized Wilkinson power divider with at least 10% bandwidth, and minimal loss, that has been fabricated using DDM techniques and materials. A similar design using traditional techniques and materials is also presented, for the sake of performance comparison.

Section 6.2 summarizes the theory of general 3-port power dividers, and the theory of operation of the the Wilkinson power divider. Section 6.3 discusses a miniaturization technique whereby the quarter wavelength transformer section of the traditional Wilkinson power divider is replaced with a capacitively loaded transformer section whose length is less than a quarter wavelength. In this section, the design equations for such a device are derived. This technique is not original, and is based on [27]. Section 6.4 presents the design and performance data of a traditionally manufactured Wilkinson power divider, fabricated on 32 mil Rogers 4003C. Finally, section 6.5 presents an almost identical design to that of 6.4, but optimized for DDM fabrication.

6.2 The Wilkinson Power Divider
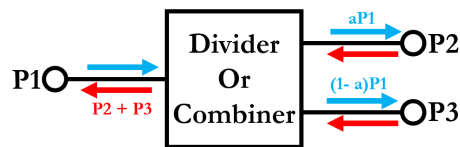
Figure 6.1 3-Port power divider or combiner.

A basic three port T-junction power divider or combiner (Figure 6.1) cannot be simultaneously matched at all ports, reciprocal, and lossless [13]. This is easily demonstrated with the application of a few simple concepts. If the network is reciprocal then $[S]$ is a symmetric matrix. If the network is matched at all ports, then $S_{ii}=0$. Under these conditions, the S-parameter matrix for the 3-port network is:

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{31} & S_{32} & 0 \end{bmatrix} \tag{6.1}$$

If a lossless condition is imposed, conservation of energy yields an inconsistency. To be lossless, $[S]$ must be unitary, which is to say:

$$\sum_{k=1}^{N} S_{ki} S_{kj}^* = \delta_{ij}, \forall\, i,j \tag{6.2}$$

where

$$\delta_{ij} = \begin{cases} 1, & i = j \\ 0, & i \neq j \end{cases}$$

Applying equation 6.2 to the matrix 6.1, the following relationships emerge:

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{6.3}$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \tag{6.4}$$

$$|S_{13}|^2 + |S_{23}|^2 = 1 \tag{6.5}$$

$$S_{13}^* S_{23} = 0 \tag{6.6}$$

$$S_{23}^* S_{12} = 0 \tag{6.7}$$

$$S_{12}^* S_{13} = 0 \tag{6.8}$$

These relationships are inconsistent, because if equations 6.6-6.8 hold, then any two of S_{12}, S_{13}, and S_{23} must be zero in which case one of equations 6.3-6.5 cannot hold. Hence, the network cannot be simultaneously matched at all ports, reciprocal, and lossless.

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Lossless reciprocal networks that are matched at all ports with isolation between the ports are desirable. In 1960 Ernest J. Wilkinson published [28] in which a special 3-port power divider design was described that exhibits all of these characteristics under specific operating conditions. The design is shown in Figure 6.2. The design utilizes a quarter wave transformer in each branch, and a resistor between the output ports. The resistor only dissipates power reflected from the output ports, so if the output ports are matched, no power is dissipated and the network *appears* lossless, if driven from port 1 [13].
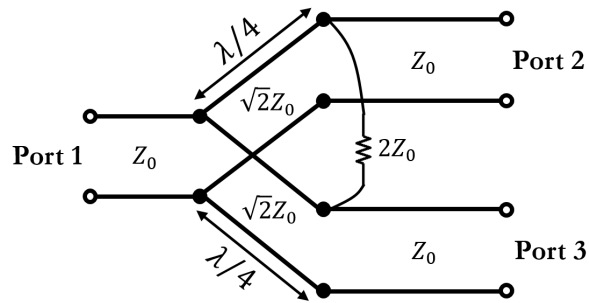
Figure 6.2 The Wilkinson power divider.

Using even and odd mode analysis, the S-parameter matrix of the Wilkinson power divider can be found to be:

$$[S] = \frac{-\sqrt{2}}{2} \begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix} \tag{6.9}$$

If the device is driven at port 1, and ports 2 and 3 are matched, then the power is equally split between ports 2 and 3, and no power is dissipated in the resistor. However, if either port 2 or 3 is driven, half of the power will appear at port 1, but the other half is dissipated by the resistor. This is shown mathematically in equations 6.10 – 6.12. Equation 6.10 satisfies the lossless condition (6.2.2), where i=j=1, but 6.11, where i=j=2, and 6.12, where i=j=3, do not.

$$|S_{21}|^2 + |S_{31}|^2 = \left(\frac{\sqrt{2}}{2}\right)^2 + \left(\frac{\sqrt{2}}{2}\right)^2 = 1 \tag{6.10}$$

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$$|S_{12}|^2 = \left(\frac{\sqrt{2}}{2}\right)^2 = 0.5 \tag{6.11}$$

$$|S_{13}|^2 = \left(\frac{\sqrt{2}}{2}\right)^2 = 0.5 \tag{6.12}$$

6.3 Capacitively Loaded Wilkinson Power Divider

In section 6.2, the classic Wilkinson power divider was presented. A notable feature of this device is the quarter wavelength sections. As frequency increases, the size of these sections decrease, but there are clearly minimum size requirements at any given frequency. At 2.45GHz, for example, $\lambda_0 = 122.4$ mm which is by no means inconsiderable. In [29] a miniaturized Wilkinson power divider is presented, whereby the lengths of the quarter-wavelength sections are reduced with the addition of shunt capacitors at the input and outputs. In microstrip designs, a secondary size reduction occurs in that the characteristic impedance of the transformer section increases as the length is further reduced, and this corresponds to a thinner trace. The general design is shown in Figure 6.3.
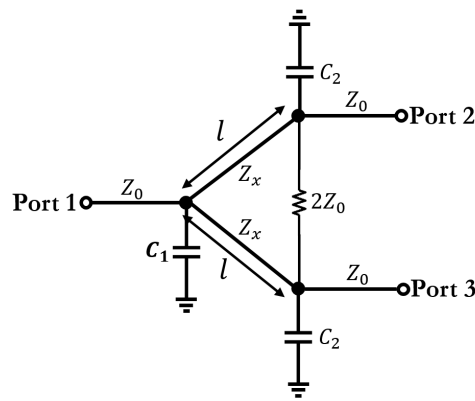
Figure 6.3 Capacitively loaded Wilkinson 3dB power divider.

[29] mentions the use of even and odd mode analysis to derive design equations for Z_x, C_1, and C_2, but a typo obscures the results. Expressions to determine the values are derived herein. To find these values, ABCD parameters are used to equate a quarter-wavelength transmission line of

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characteristic impedance Z_Q with a length of transmission line of length l and characteristic impedance Z_x, with a shunt capacitor at the input and output. This is depicted in Figure 6.4. Table 6.1 [13] gives the relevant ABCD parameters.

$$\begin{bmatrix} A_Q & B_Q \\ C_Q & D_Q \end{bmatrix} = \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix}\begin{bmatrix} A_x & B_x \\ C_x & D_x \end{bmatrix}\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix}$$
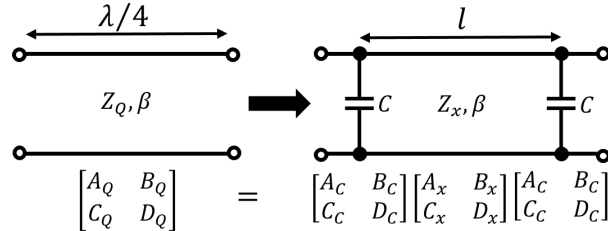
Figure 6.4 Depiction of the procedure to find expressions for Z_x, C_1, and C_2.

Table 6.1 ABCD parameters for an ideal transmission line and an admittance.

Circuit	ABCD Parameters	
l z_0, β	$A = \cos(\beta l)$ $C = jY_0 \sin(\beta l)$	$B = jZ_0 \sin(\beta l)$ $D = \cos(\beta l)$
Y	$A = 1$ $C = Y$	$B = 0$ $D = 1$

Using Table 6.1, the following ABCD matrices are calculated:

$$\begin{bmatrix} A_Q & B_Q \\ C_Q & D_Q \end{bmatrix} = \begin{bmatrix} 0 & jZ_Q \\ jY_Q & 0 \end{bmatrix} \tag{6.13}$$

$$\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \tag{6.14}$$

$$\begin{bmatrix} A_x & B_x \\ C_x & D_C \end{bmatrix} = \begin{bmatrix} 0 & jZ_x \\ jY_x & 0 \end{bmatrix} \tag{6.15}$$

so, multiplying [(6.14)][(6.15)][(6.14)] yields

$$\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix}\begin{bmatrix} A_x & B_x \\ C_x & D_x \end{bmatrix}\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} =$$

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$$\begin{bmatrix} \cos(\beta l) - \omega C Z_x \sin(\beta l) & jZ_x\sin(\beta l) \\ jY_x\sin(\beta l) + 2j\omega C\cos(\beta l) - j(\omega C)^2 Z_x\sin(\beta l) & \cos(\beta l) - \omega C Z_x\sin(\beta l) \end{bmatrix} \quad (6.16)$$

To find the values of Z_x, C_1, and C_2, (6.16) is equated to (6.13) which results in the following set of equations:

$$\cos(\beta l) - \omega C Z_x\sin(\beta l) = 0 \quad (6.17)$$

$$jZ_x\sin(\beta l) = jZ_Q \quad (6.18)$$

$$jY_x\sin(\beta l) + 2j\omega C\cos(\beta l) - j(\omega C)^2 Z_x\sin(\beta l) = jY_Q \quad (6.19)$$

Rearranging (6.17) and (6.18) yields

$$\cos(\beta l) = \omega C Z_x\sin(\beta l) \quad (6.20)$$

$$Z_x = \frac{Z_Q}{\sin(\beta l)} \quad (6.21)$$

which can be substituted into (6.19) to yield

$$jY_x\sin^2(\beta l) + 2(\omega C)^2 Z_x\sin(\beta l) - j(\omega C)^2 Z_x\sin(\beta l) = jY_Q \quad (6.21)$$

which reduces to

$$\omega C = \sqrt{\frac{1 - sin^2(\beta l)}{Z_Q^2}} \quad (6.22)$$

from which an expression for C is

$$C = \frac{\cos(\beta l)}{\omega Z_Q} \quad (6.23)$$

In these expressions, Z_Q is the characteristic impedance of the quarter wave transformer transmission line section in the classical Wilkinson power divider, which is equal to $\sqrt{2}Z_0$. Equation 6.23 is an expression which finds the appropriate value of C for a single branch of the power divider. Since there are two branches in the power divider, who share a single input, there should be two parallel capacitors of equal value at the input. This, of course, is simplified by simply using a single capacitor, C_1, whose value is twice that of the output capacitor, C_2.

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From this analysis, a set of simple design equations emerge. For a given transformer section length, l, the design equations for the capacitvely loaded Wilkinson power divider are:

$$C_2 = \frac{\cos(\beta l)}{\omega\sqrt{2}Z_0} \qquad (6.24)$$

$$C_1 = 2C_2 \qquad (6.25)$$

$$Z_x = \frac{\sqrt{2}Z_0}{\sin(\beta l)} \qquad (6.26)$$

6.4 Traditional PCB Version (Rogers 4003C)

In this section, a 4-way, 6dB, capacitively loaded Wilkinson power divider constructed using traditional subtractive manufacturing techniques is considered. The device is fabricated on Rogers 4003C, with a 32 mil dielectric and 1oz copper cladding. The LPKF S63 is used for milling the board. In order to prevent the over-milling of the substrate, the conductive trace outlines are milled, and the unwanted copper is removed by simply peeling it away. This technique maintains the perfect 32mil dielectric thickness over the majority of the circuit.

Table 6.2 Line widths for lines of various characteristic impedances. 32mil Rogers 4003C and ABS substrates.

Length	Z_x	W_{Cu} (mm)	W_{CB028} (mm)
$\lambda/4$	70.7	0.95	1.24
$\lambda/6$	81.7	0.70	0.93
$\lambda/8$	100	0.42	0.59
$\lambda/10$	120.3	0.23	0.36
$\lambda/12$	141.4	0.12	0.20

The device is miniaturized using the capacitive loading technique discussed in section 6.3. Since this thesis is principally concerned with DDM RF devices, the extent to which the device could be miniaturized is ultimately governed by the limitations of that technology. Table 6.2 gives the line widths of the transformer sections for their associated characteristic impedances, for lines of both copper and CB028. A transformer section length of $\lambda / 8$ is used, which affords practical line

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widths for both the S63 milling and the SmartPump™ that is used for printing conductive traces. According to [29], this may provide up to a 57.5% area reduction from the traditional $\lambda / 4$ transformer section.

In order to achieve an equal 6dB power split, three 3dB dividers are used in a corporate network configuration. The design consists of a 3dB splitter with an identical 3 dB splitter at each output port. This is shown conceptually in Figure 6.5. Equations 6.24, 6.25, and 6.26 yield the following ideal component values, based on a 50Ω system impedance:

$$C_1 = 1.3 \, pF \qquad\qquad C_2 = 0.65 \, pF \qquad\qquad Z_x = 100 \, \Omega$$

Optimization of the design in Keysight's Advanced Design System using Modelithics models for ATC 600S series capacitors results in the following final capacitor values:

$$C_1 = 1.0 \, pF \qquad\qquad\qquad C_2 = 0.6 \, pF$$

Figure 6.6 shows the fabricated first stage. In order to take 2-port measurements, a 50Ω narrow band load is connected to port 3. Figure 6.7 shows comparisons of measured and simulated performance. Table 6.3 gives the pertinent numerical data at 2.45 GHz. For these designs ATC 600S capacitors and KOA Speer RK73H resistors are used.

The 3 dB splitter described above is duplicated at each output, to form the schematic layout shown in Figure 6.8. Figure 6.9 shows the fabricated circuit. The area of the circuit footprint is 394.8mm^2.

In order to take 2-port measurements, three of the output ports are terminated in designed narrow band 50Ω loads. Simulation data for isolation, return loss, and insertion loss at each ideally terminated port is shown in Figure 6.10. Figure 6.11 compares the ideally terminated and designed load terminated simulations with measurement data, and the pertinent numerical values are summarized in Table 6.4. These results show a design that has good isolation between all ports, and far greater than 10% bandwidth in the insertion loss and return loss at the input and output. This

design has an optimal performance frequency lower than 2.45GHz. The best insertion loss and isolation are not at the same frequency in the capacitively loaded Wilkinson power divider, so when designing such a device, there are some trade-offs. [29] predicts this offset, claiming that for a $\lambda / 12$ long transformer section, the frequency difference is 1.5GHz. The notion that this result is an effect of an impedance mismatch at port one, when terminated for the isolation measurements, is discredited, and rather attributed to the parasitic effects of the thin film resistor at the output ports. The results show good agreement between measured and simulated data.

Figure 6.5 Capacitively loaded 6dB Wilkinson power divider.
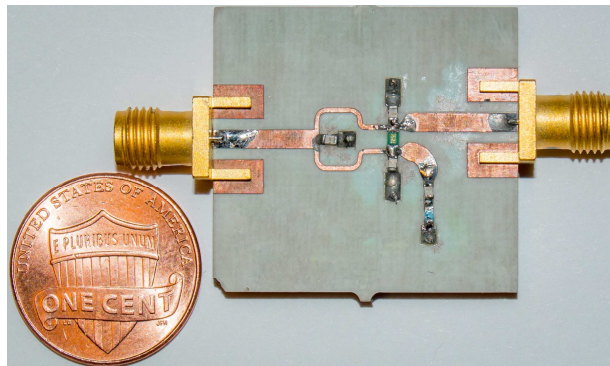
Figure 6.6 Capacitively loaded 3dB Wilkinson power divider, fabricated on 32 mil Rogers 4003C.

Figure 6.7 Rogers 4003C stage 1 (3dB) measurement and simulation data. (i) S11 & S22. (ii) S21.

Table 6.3 3dB Wilkinson power divider on Rogers 4003C.

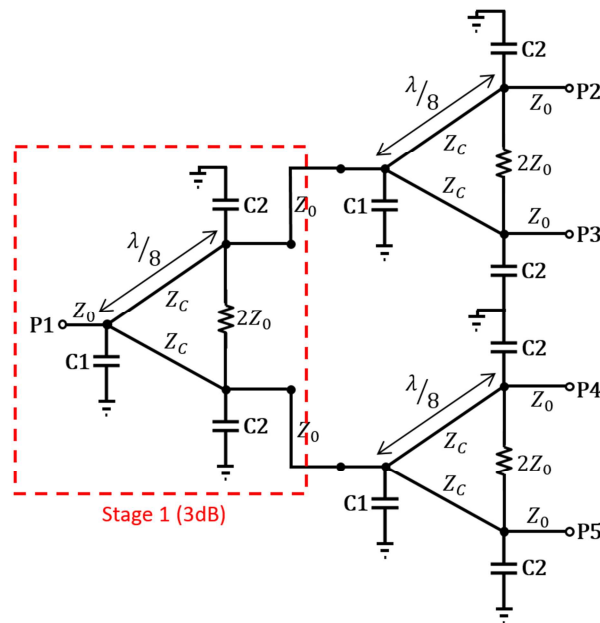| $f_c=2.45GHz$	Input Return Loss		P2 Insertion Loss		Output Return Loss (dB)	
	(dB)	>10 dB Bandwidth (%)	(dB)	+ 0.1 dB Bandwidth (%)	(dB)	10 dB Bandwidth (%)
Simulated	25.8	41.2	3.1	18.0	40.0	93.1
Measured	21.9	43.6	3.5	26.1	21.9	94.7
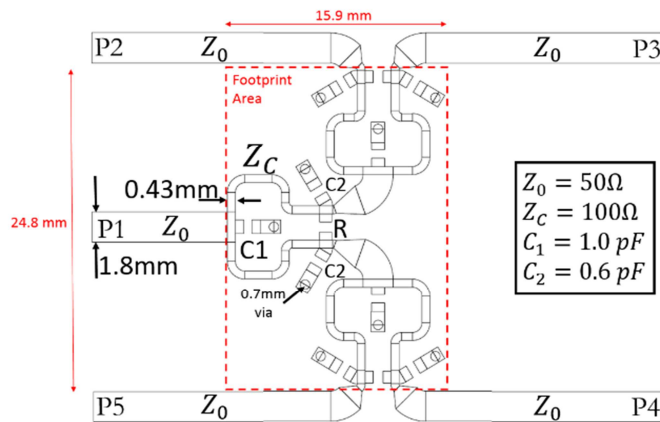
Figure 6.8 Capacitively loaded 6dB Wilkinson power divider schematic.
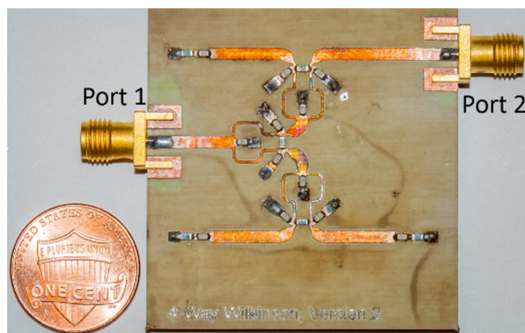
Figure 6.9 Capacitively loaded 6dB Wilkinson power divider, fabricated on 32 mil Rogers 4003C.
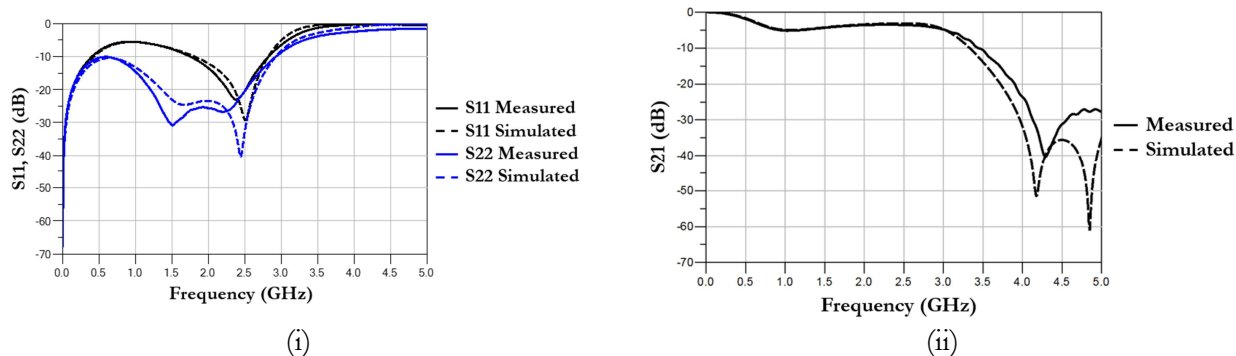
Table 6.4 6dB Wilkinson power divider on Rogers 4003C.

f_c=2.45GHz	Input Return Loss		P2 Insertion Loss		Output Return Loss (dB)	
	(dB)	>10 dB Bandwidth (%)	(dB)	+0.1 dB Bandwidth (%)	(dB)	10 dB Bandwidth (%)
Simulated (ideal terminations)	15.6	53.6	6.3	44.9	23.7	94.2
Simulated (designed terminations)	19.1	54.7	6.3	51.0	25.3	98.4
Measured	19.3	58.4	6.6	50.2	25.0	104.9

(i)

(ii)

(iii)
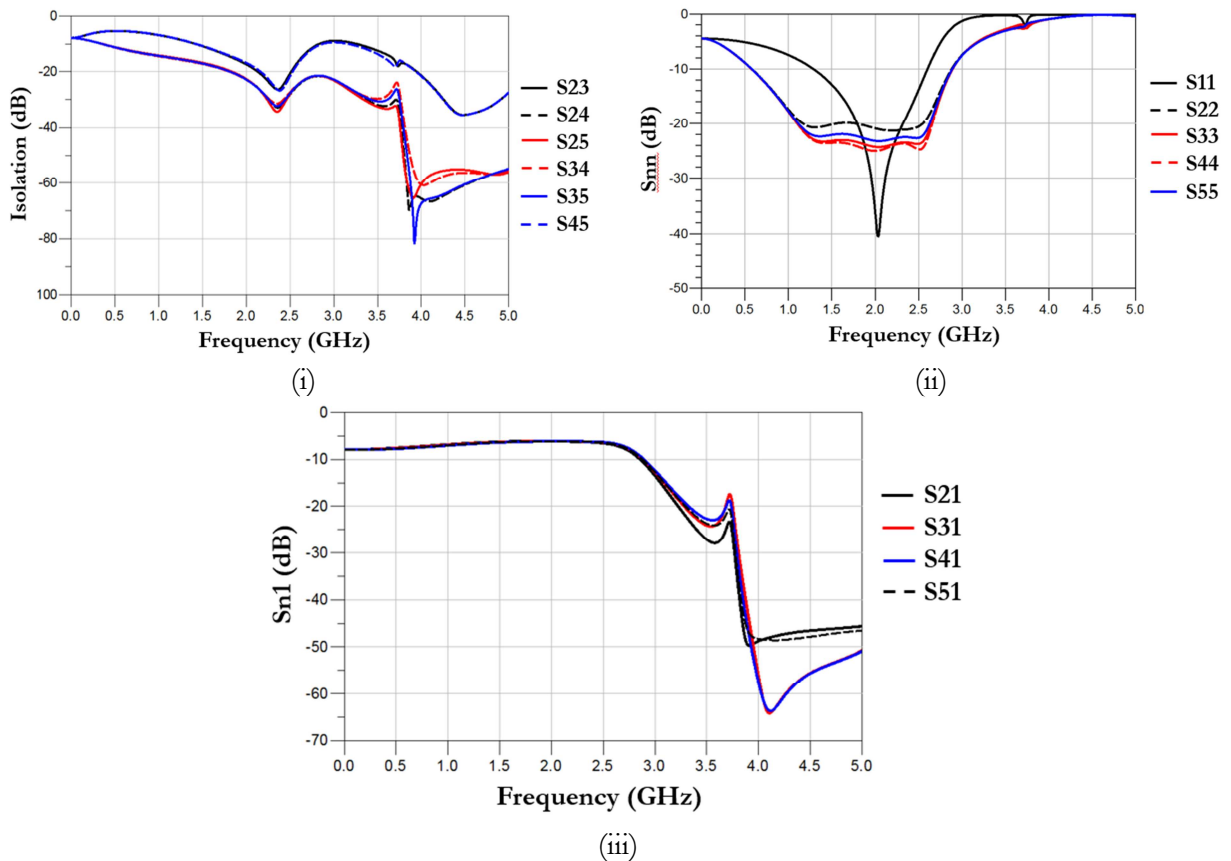
Figure 6.10 Simulation plots with ideal terminations at each port, Rogers 4003C. (i) Isolation. (ii) Return loss. (iii) Insertion loss.
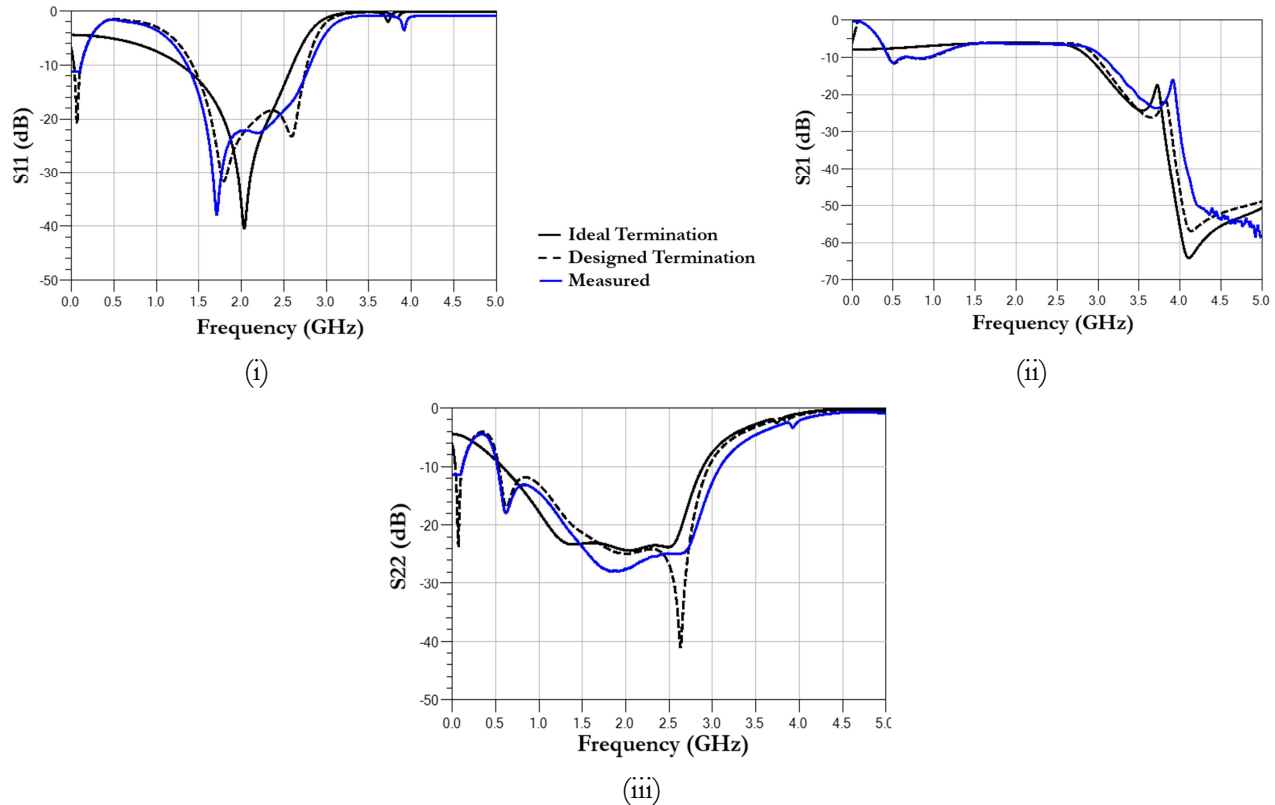
Figure 6.11 Simulated and measured S-parameters of 6dB Wilkinson power divider fabricated on 32 mil Rogers 4003C. (i) S11. (ii) S21. (iii) S22.

6.5 DDM Version

The design described in section 6.2 is modified for fabrication on a 32 mil ABS substrate, and CB028 conductive traces. Since ABS has a lower dielectric constant then Rogers 4003C ($\epsilon_{r,ABS} \approx 2.58$, $\epsilon_{r,4003C} \approx 3.55$) the line width for a line of a given characteristic impedance is higher. Since the Rogers 4003C design was left shifted in almost all measured and simulated parameters, this DDM design is optimized more for insertion loss and return loss at 2.45 GHz than isolation. Shifting these parameters up in frequency, as compared to the Rogers 4003C version, shifts the optimum isolation frequency up also, as expected. The significant modification here is the value of C_1, which is 0.8 pF in this design, but 1.3 pF in the Rogers 4003C design. This deviates from the theory quite significantly, since the theory dictates that $C_1 = 2C_2$, but in this design

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C_1=1.3C_2. A better optimization strategy would likely have reduced this discrepancy, but the target specifications are met, regardless.

Figure 6.12 shows the first stage device, with port 3 terminated in a narrow band 50Ω designed load. Figure 6.13 shows the simulated and measured data for the first stage. It is clear from this plot at low frequencies, the measured data follows closely the simulated data, but as the frequency increases, the measurement data becomes right shifted with respect to the simulation data. Table 6.5 gives the pertinent numerical data, at 2.45GHz. Potential causes for this frequency shift are discussed later in this section.
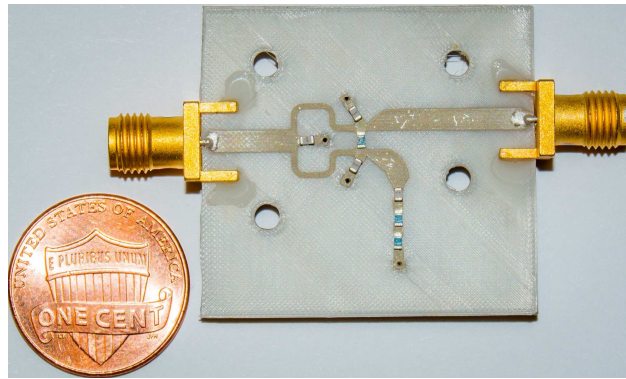
Figure 6.12 DDM fabricated 3dB Wilkinson power divider. Stage 1.
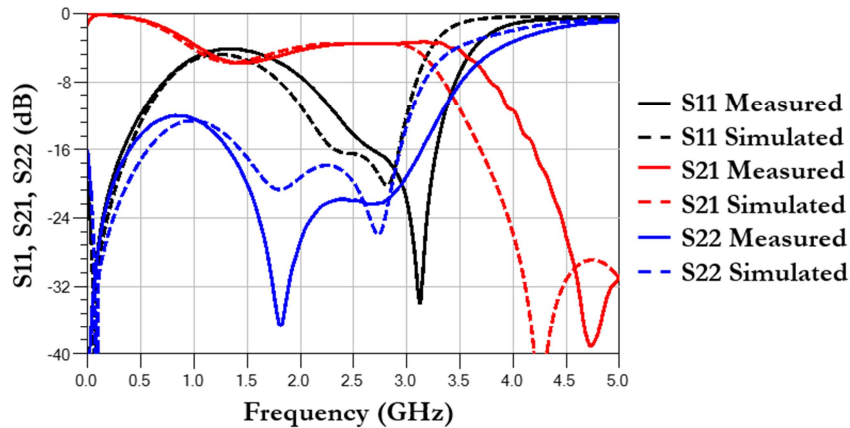
Figure 6.13 DDM fabricated 3dB Wilkinson power divider S-parameters.

Table 6.5 3dB DDM fabricated Wilkinson power divider.

f_c=2.45GHz	Input Return Loss		P2 Insertion Loss		Output Return Loss (dB)	
	(dB)	>10 dB Bandwidth (%)	(dB)	+ 0.1 dB Bandwidth (%)	(dB)	10 dB Bandwidth (%)
Simulated	17.9	44.5	3.5	31.8	19.4	125.7
Measured	13.6	47.8	3.5	42.9	22.0	138.8

The layout schematic for the 4-way DDM fabricated device is given in Figure 6.14, and a photograph of the fabricated device is shown in Figure 6.15. The area of the device footprint is 401.7 mm², which is 1.6% larger than the Rogers 4003C design. This negligible difference is due to the wider lines. As with the Rogers 4003C design, ports 3, 4, and 5 are terminated in a narrowband 50Ω load. The isolation, insertion loss, and return loss at each port are simulated with ideal terminations, and the results are shown in Figure 6.16.
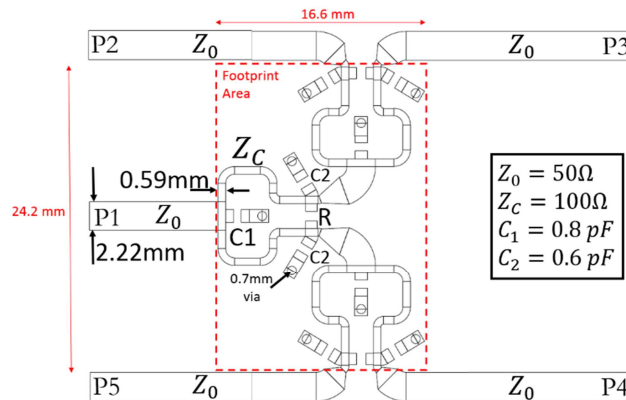
Figure 6.14 Capacitively loaded 6dB Wilkinson power divider schematic.
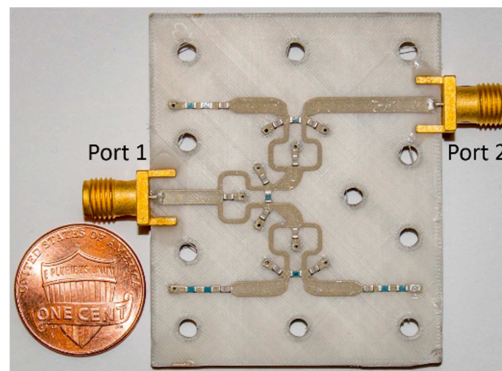
Figure 6.15 DDM fabricated capacitively loaded 6dB Wilkinson power divider.

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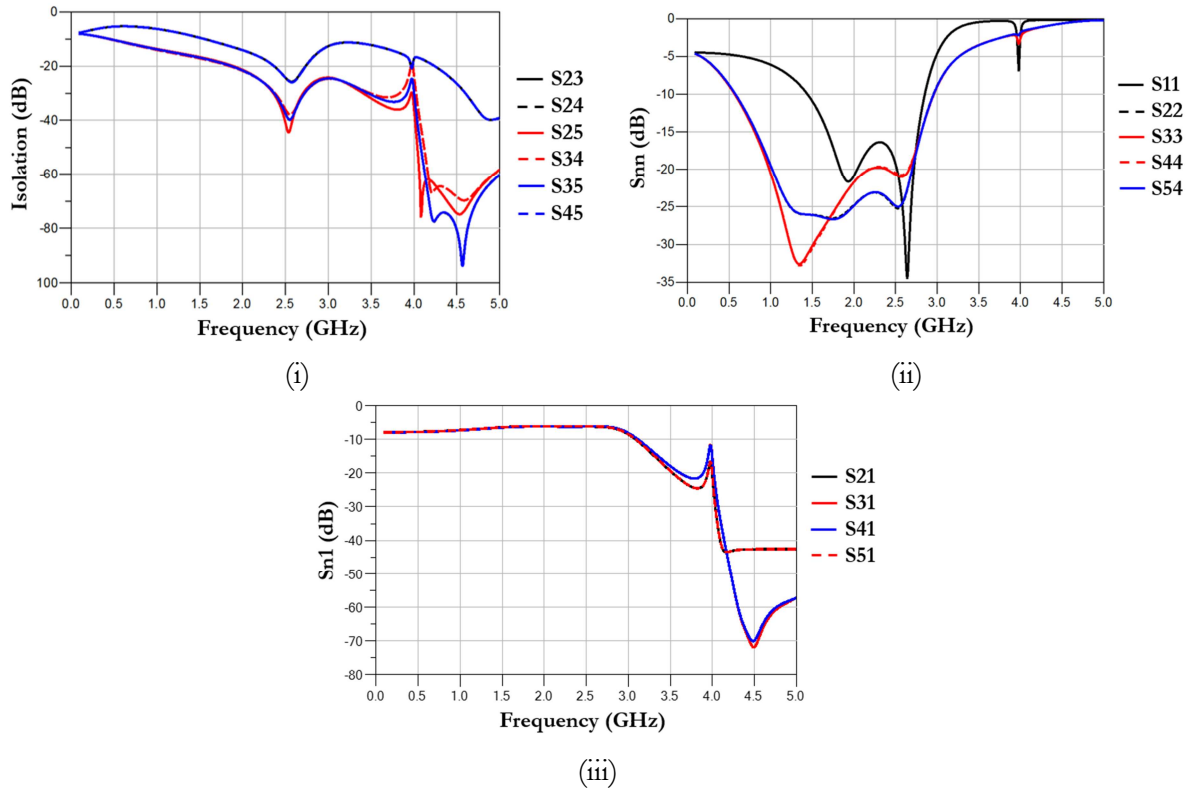
Figure 6.16 Simulation plots with ideal terminations at each port, DDM fabricated. (i) Isolation. (ii) Return loss. (iii) Insertion loss.

Figure 6.17 compares the ideally terminated and designed load terminated simulations with measurement data, and the pertinent numerical values are summarized in Table 6.6. Although the design specifications are met in the simulated and measured data, there are again some discrepancies between measured and simulated data.

The measured data and designed termination simulation data are similar, but the measured data is shifted up by around 300 MHz in frequency at higher frequencies. This effect has several potential causes, and is a notable deviation from the Chapter 4 predictions. The dielectric constant used for the purposes of simulation was 2.58. This is an estimation based on [30]. It is possible that this value is lower in reality, since a 3D printed part potentially has small air pockets inside of it. Lowering the dielectric constant will cause a positive frequency shift. An extreme case, with $\epsilon_r =$

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2.0, was simulated, and the shift was reduced to around 170 MHz, but other artifacts were introduced. The S11 plot of this change is shown in Figure 6.18(i).

Another cause of discrepancy is the accuracy of the dimensions in fabricated device. The 32mil substrate was measured to be around 30mil in reality, and the line widths are relatively close to the design values, but they are inconsistent. The simulated effect of this is shown in Figure 6.18 (ii). Figure 6.19 shows photographs of 50Ω and transformer section traces at 4X magnification, and the dimensions at various points are overlaid. This shows that the transformer section, which has a design width of 0.59mm has actual widths up to 0.65mm. This difference is minor, but it is possible that the non-uniformity is causing unexpected results. An increased transformer section width reduces the impedance of the line, which according to equation 6.26, for a line with an electrical length less than or equal to 90 degrees, causes a positive frequency shift.
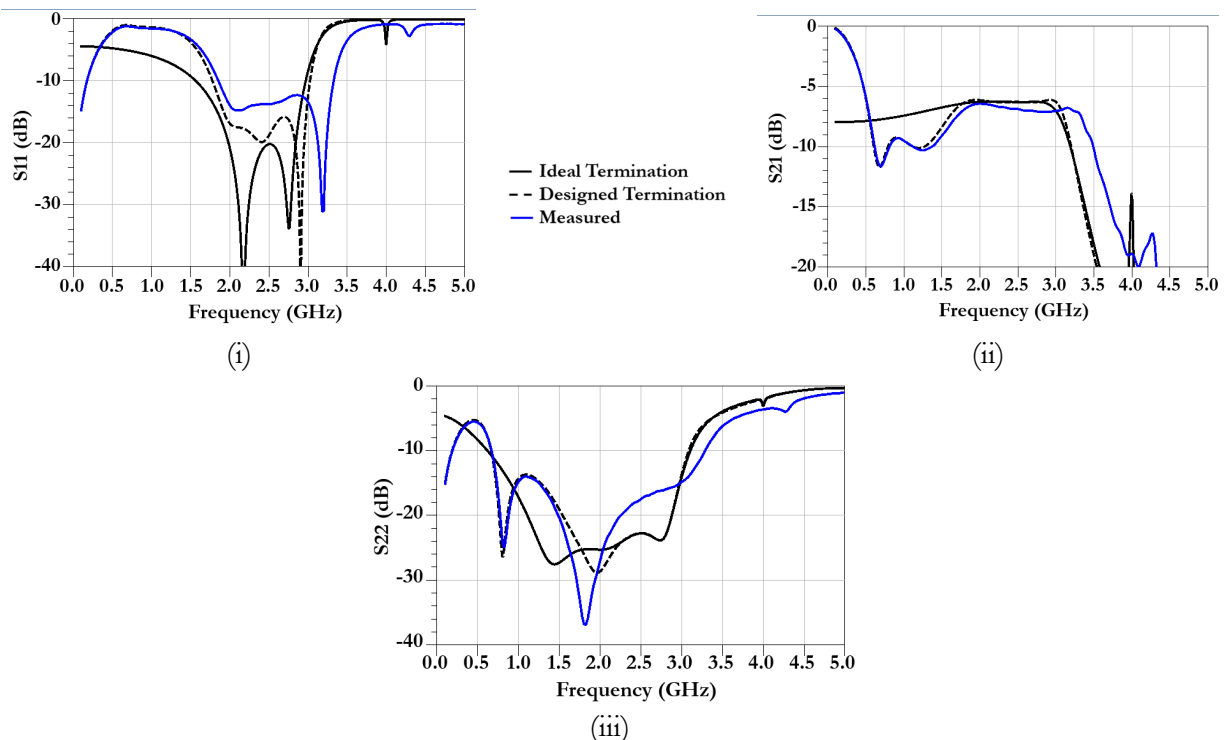
Figure 6.17 Simulated and measured S-Parameters of the DDM fabricated 6dB Wilkinson power divider. (i) Input return loss. (ii) Insertion loss. (iii) Output return loss.

Table 6.6 6dB DDM fabricated Wilkinson power divider.

f_c=2.45GHz	Input Return Loss		P2 Insertion Loss		Output Return Loss (dB)	
	(dB)	>10 dB Bandwidth (%)	(dB)	+ 0.1 dB Bandwidth (%)	(dB)	10 dB Bandwidth (%)
Simulated (ideal terminations)	20.6	57.1	6.3	49.4	22.9	112
Simulated (designed terminations)	19.7	50.6	6.9	50.2	22.9	98.4
Measured	13.8	60	6.9	31.8	17.9	106.5

Figure 6.18 (i) Re-simulated S11 with $\epsilon_r = 2.0$. (ii) Re-simulated with 30 mil substrate.

Figure 6.19 Print dimensions. (i) 50Ω line. (ii) Transformer section.

6.6 Conclusion

The purpose of this chapter was to build a 4-way miniaturized Wilkinson power divider using DDM techniques and materials, with a bandwidth of 10% and minimal loss. This was achieved, although there are some discrepancies between simulation and measured data. It was suggested that these discrepancies are due to fabrication tolerances and ambiguities in material parameters.

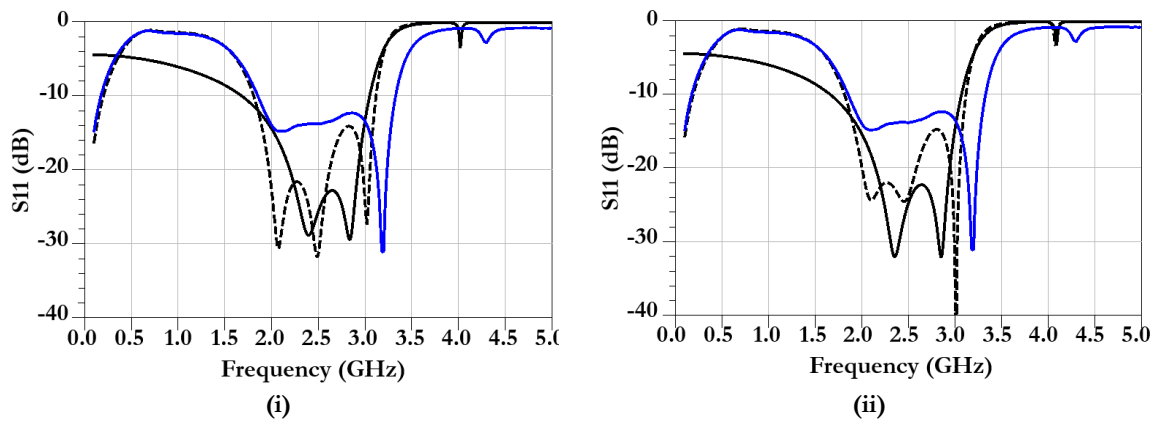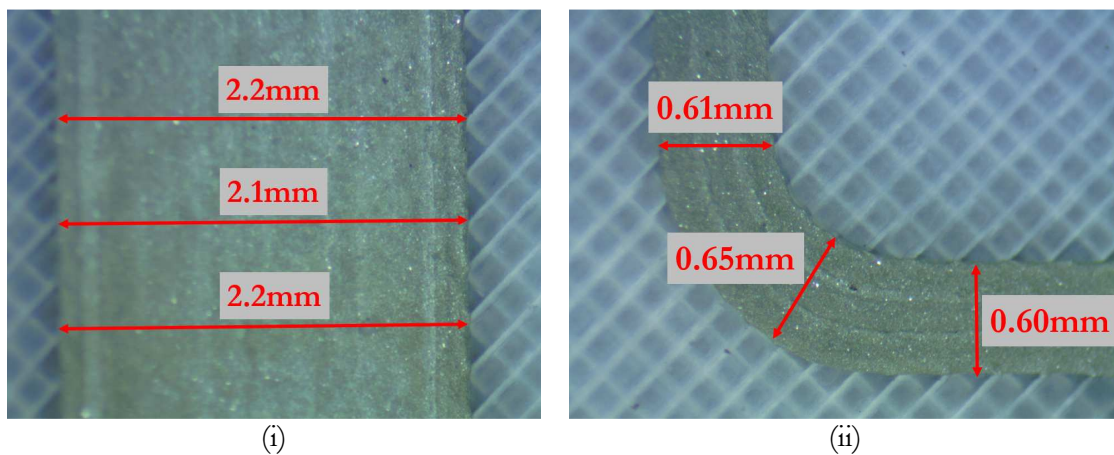Comparing the DDM results to the Rogers 4003C results, there is not a significant reduction in performance between the two technologies. The DDM materials are lossier in both the dielectric substrate and the conductive traces than Rogers 4003C, so the 0.3dB increase in the insertion loss is expected, and tolerable.

Considering Chapter 4, and the effect of the ripple orientation on performance, there is potential to optimize this, and similar, designs. In this design, the orientation of the surface ripple with respect to the traces is not consistent. The prints analyzed in this chapter have a surface ripple that is at 45° with respect to the input and output 50Ω lines, so clearly this is not the case for most of the other lines. The ability to design the surface ripple direction for each section of transmission line would be of some benefit.

The work in this chapter was assigned a clearance of CLEARED on October 8, 2015 (Case Number: 88ABW-2015-4858).

CHAPTER 7: CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusion

This thesis has focused on RF/microwave packaging fabricated using DDM techniques and materials. It has been demonstrated, in Chapter 4, that although these materials are quite lossy as compared to Rogers 4003C, they perform adequately, and can sustain relatively high power RF inputs, over extended periods of time, repeatedly. This is a pleasing result, and demonstrates a critical component of the suitability for electronics packaging.

It has also been demonstrated that these materials and techniques are capable of incorporating IC devices, although there are some limitations with respect to how this is achieved. Specifically, the manual application of epoxy and placing of IC devices is not ideal, and does not achieve repeatable results. IC devices that have thermal management requirements have not been ruled out, but further research in this area is needed. A thermal management technique that mirrors industry standard methods was employed, and temperatures above the GTC of ABS were sustained, with no degradation to the ABS. Again, this is a pleasing result.

Finally, it has been demonstrated that this technology is suitable for passive RF/microwave electronics. Chapter 6 presented a 6dB Wilkinson power divider, with large bandwidth, and only marginally lower loss than a similar Rogers 4003C design. This design incorporated passive surface mount components, specifically capacitors, and thus it is further demonstrated that components may be secured to a DDM package, electrically and mechanically.

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7.2 Recommendations for Future Work

As stated above, further research into thermal management techniques is recommended. While it has been demonstrated that high temperatures can be sustained without damage to the packaging materials, the power amplifier device became much hotter than recommended. H20E was used for a thermal via in this case, but H20E-HC or DuPont's CB100 may be better choices. H20E-HC has a higher thermal conductivity than H20E. DuPont do not list thermal conductivity of CB100 on the data sheet, it is advertised for this exact purpose.

It would also be interesting to extend the design of the capacitively loaded Wilkinson power divider. The design presented here used surface mount capacitors, but this technology lends itself to a potentially better solution. Re-designing the power divider with printed metal-insulator-metal (MIM) capacitors could potentially improve the performance since the manual epoxying of the component to the board would no longer be necessary. The potential for this technique is a benefit of the DDM process over traditional PCBs where the control of layer thicknesses is often not possible.

Another recommendation is a much deeper study of the effect of the ABS surface ripple on performance. The results presented here were somewhat inconclusive since measurements did not match the simulations. A significant difference between the simulations and measurements is the inclusion of the SMA connector, and the manual epoxying of it to the board. Given the minimal simulated difference in performance between ripple orientations, this study is perhaps better suited to probing based measurements.

A final recommendation is the extension of the thermal response of transmission lines to various transmission line types, and substrate thicknesses. This thesis presented an analysis of a single design, but a much broader analysis would yield much more conclusive results.

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